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Properties and Transistor Applications of Silicon Nanowires

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Abstract

This paper describes the characteristics of silicon nanowires (SiNW) and their use in sensors technology by existing literature. An introductory part talks about nanowires in general and how they can affect the evolution of next generation sensors technology . The properties of silicon nanowires describe their mechanical, electrical, chemical, optical and thermal properties.

1. INTRODUCTION

Nanowires can be defined as nanostructures which have diameters towards the nanometerscale (in the area of tens of nanometers). It is possible to make conducting (e.g. Ni, Pt, Au), semiconducting (e.g. Si, InP, GaN) and insulating (e.g. SiO2, TiO2) nanowires which can finddifferent possible real applications [16]. The basic methods for the synthesis of nanowires arethe bottom-up method and the top-down method which is similar to lithography [1, 16]. The bottom-up method is based on chemical composition and is the preferred method for the nanowires' synthesis because important parameters of a nanowire such as radius, length, doping levels, chemical composition and growth direction can be controlled accurately [4, 14,16].

Silicon nanowires are considered as popular nanomaterials due to their exceptional electrical and mechanical properties [5]. They are semiconducting nanowires and their conductivity can be controlled by the field-effect action [3, 16, 17]. For this reason, silicon nanowires can be used probably for the next generation of field-effect transistors and advanced sensors [7, 9].

2. PROPERTIES OF SILICON NANOWIRES

- Mechanical properties

It is expected that nanowires, which are 1-D systems, have interesting mechanical properties due to their high aspect ratio compared to bulk materials and the reduced

number ofdefects per unit length [4, 12]. However, manipulating these materials for mechanical measurements is a challenging task [4, 6]. The main methods which are used to investigate their mechanical properties are mechanical resonant, the Atomic Force Microscope (AFM) and nanoindentation [5, 6]. The resonant method is used only for the determination of the elastic properties and it is not easy to measure the applied force accurately when using the AFM method. On the other hand, nanoindentation has very good force and displacement resolution and control [6].

Nanowires can be used in the field of sensors and nano-electromechanical systems (NEMS) [4, 5]. This is because, according to their tensile strength and Youngs Modulus, theyare very robust materials and have the ability to store elastic energy [4, 11]. In addition, nanoscale resonators can be built by silicon nanowires with high oscillating frequencies (100 MHz up to 1 GHz) due to their excellent elastic properties [4, 5].

- Electrical properties

It is important to understand the electrical properties of semiconducting nanowires because they determine the suitability of silicon nanowires to be used in electronics and sensorapplications.

The large surface-to-volume ratio of nanowires makes their conductivity very sensitive to surface excitation by external charges [9, 11, 12]. As it is seen in figure 1, a small surfaceperturbation can influence the 'bulk' of a nanowire while in the case of a planar device only afraction of its surface is influenced. This important property allows the detection of a single molecule and the use of silicon nanowires in biosensors [7, 8, 11, 17].

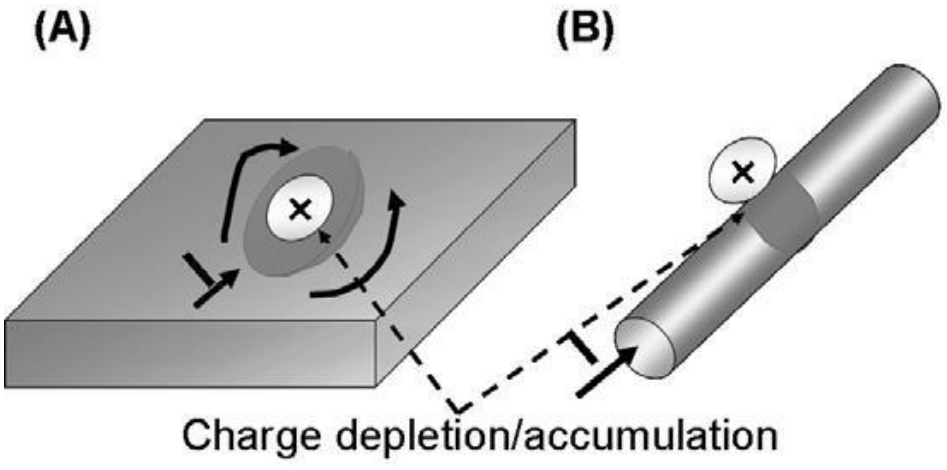

Figure 1: The major advantage of 1-D nanostructures (B) over 2-D thin film (A). Binding to 1-D nanowire leads to depletion or accumulation in the "bulk" of the nanowire as opposed to only the surface in 2-D thin-film case [11].

In addition to this, other unique properties such as quantum confinement effects and low leakage currents make nanowires attractive for the next generation of electronics and nanosystems [4, 9].

- Chemical properties

An important chemical reaction, which makes silicon nanowires very useful in sensor and transistor applications, is the natural oxidation. This is an unavoidable effect which createsoxygen-derived defects on the surface of a pure semiconductor nanowire core. It was shown, by experimental measurements, that the hole mobility of a silicon nanowire can be increased by a magnitude of two if there is proper chemical modification of the SiOx layer [1].

- Optical properties

Nanowires can exhibit mechanical strain effects if exposed to light which has a wavelength comparable to their energy bandgap. This is due to their photoelastic properties[5].

- Thermal properties

Silicon nanowires, when used within applications or experiments, may have a curved like shape and not be straight. The phonon transport can be affected by their curvature and thustheir thermal conductivity changes. The nanowire curvature is a mean of impedance to the phonon transport because phonons deviate from the main heat flow direction which flows axially through the nanowire. Therefore, thermal conductivity is reduced when the radius of the nanowire curvature decreases [2]. The effect of the curvature on the thermal impedance hasgreater effect when the radius of the curvature is one order smaller than the phonon mean-freepath (MFP) [2, 15].

This observation is interesting since the thermal conductivity of silicon nanowires can be controlled by proper shaping of the wire [2]. This is important in the use of silicon nanowiresin next generation electronics because the shrinking of electronic devices towards the nanoscale region demands an increase in power dissipation per unit area [15].

3. TRANSISTOR APPLICATIONS OF SILICON NANOWIRES

Silicon transistor technology, especially MOS technology, is scaling down as predicted by Moore's Law [4]. Initially, transistors had a 3-D active region (bulk silicon substrate) whichreduced to 2-D (ultrathin-film silicon-on-insulator (SOI)) as shown in figure 2. Recently, thetransistor active region was scaled to 1-D (FinFET on SOI) [12].

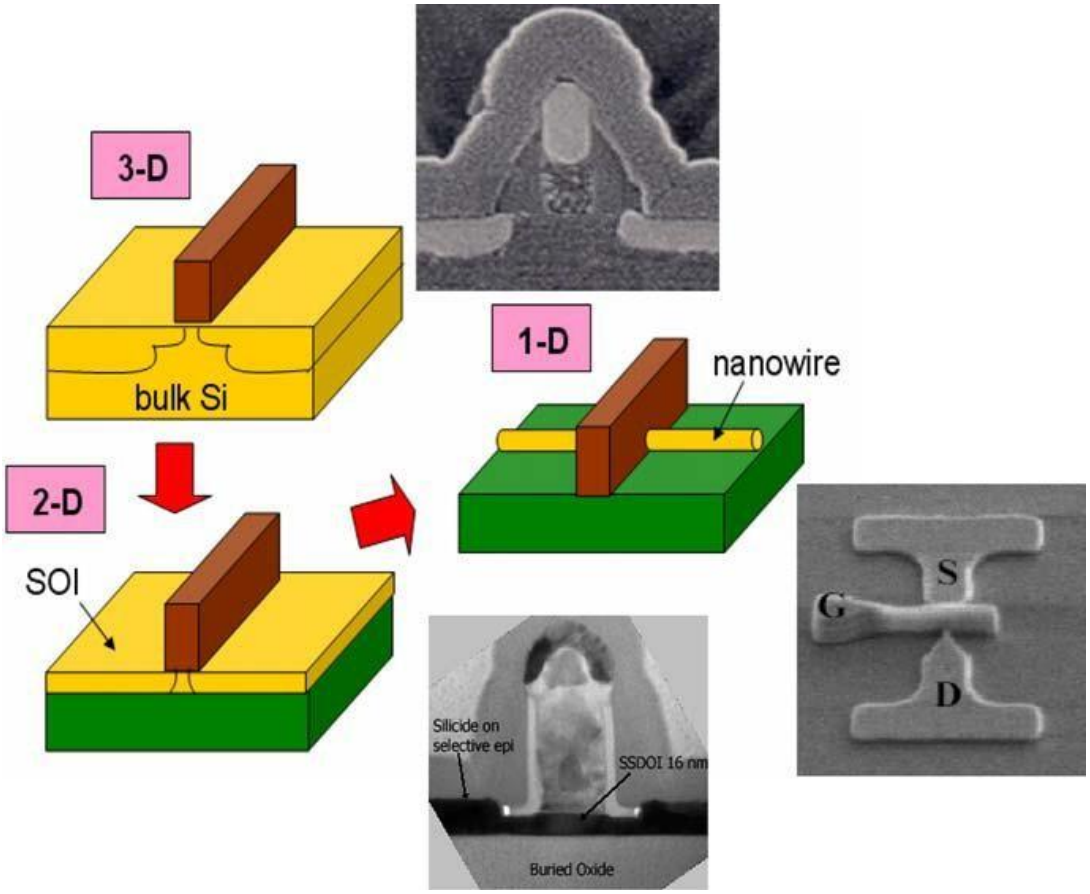

Figure 2: Continued scaling of silicon CMOS transistor into nanometer regime requires thecorresponding reduction of device active layer dimensionality [12].

One dimension structures (1-D) are the smallest structures which can be used for efficient transport of electrons [10, 11, 12]. Semiconducting nanowires belong to this categoryand they are candidates to replace the ultrathin-film SOI transistors. The reasons are that they can be manufactured in large quantities with almost identical characteristics as required by VLSI systems and because they can be manufactured using the bottom-up method rather than the top-down [14]. Bottom-up method advantages over the top-down method include well controlled device dimensions and channel width, very low power dissipation, high integration density, cheap self-assembly technology and enhanced carrier mobility due to reduced scattering (more perfect structure) and even electrical integrity [12, 14]. Silicon nanowires havebeen studied more and are referred as the most suitable for the implementation of nanowire transistors because silicon dominates the semiconductor industry and because their structure and doping can be controlled accurately [14].

Silicon nanowire transistor implementation-operation

A simple silicon nanowire transistor can be built as shown in figure 3. The two gold cubes labeled with S and D (figure 3.A) represent the source (S) and drain (D) contactsof the transistor respectively. The dark blue cylinder represents the nanowire which is thechannel of the transistor. The channel can be doped p-type or n-type. The gate of the transistoris shown in figures 3.B-C as a rectangular like plate labeled with G. The gate can be placed in a semi-cylindrical shape on the top of the nanowire or all around the the nanowire [14].

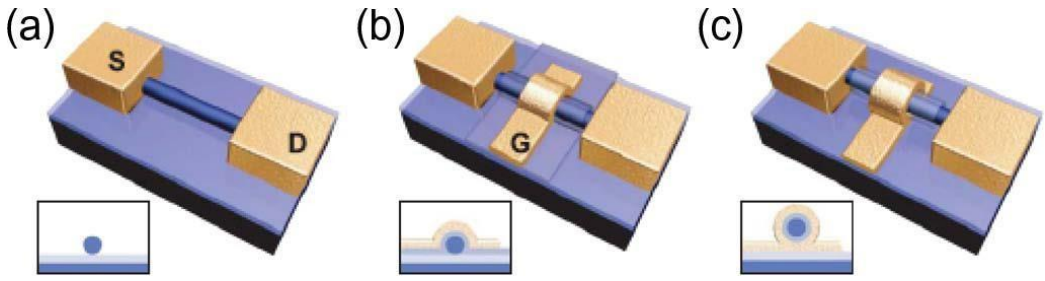

Figure 3: Schematic of NWFETS with (a) back gate, (b) semicylindrical top gate, and (c) cylindrical gate-all-around configurations. The nanowire is dark blue, gate-dielectric is light purple,and source (S), drain (D), and top-gate (G) electrodes are gold. Insets show device cross section at midpoint between source and drain [14].

SiNW transistors can find numerous real applications such as displays, data storage, 3-D computing, lasers, smart cards, wearable electronics, high efficiency programming, ring oscillators etc [12, 13, 14]. Some of them are summarized below.

- Memory array

The memory array shown in figure 4 is based on vertically grown SiNWs.

The unique array architecture and small cell size may provide high density memory at low fabrication cost with fast programming or accessing capability. Also, the speed to density ratiois higher while the cost to density ratio is lower [12].

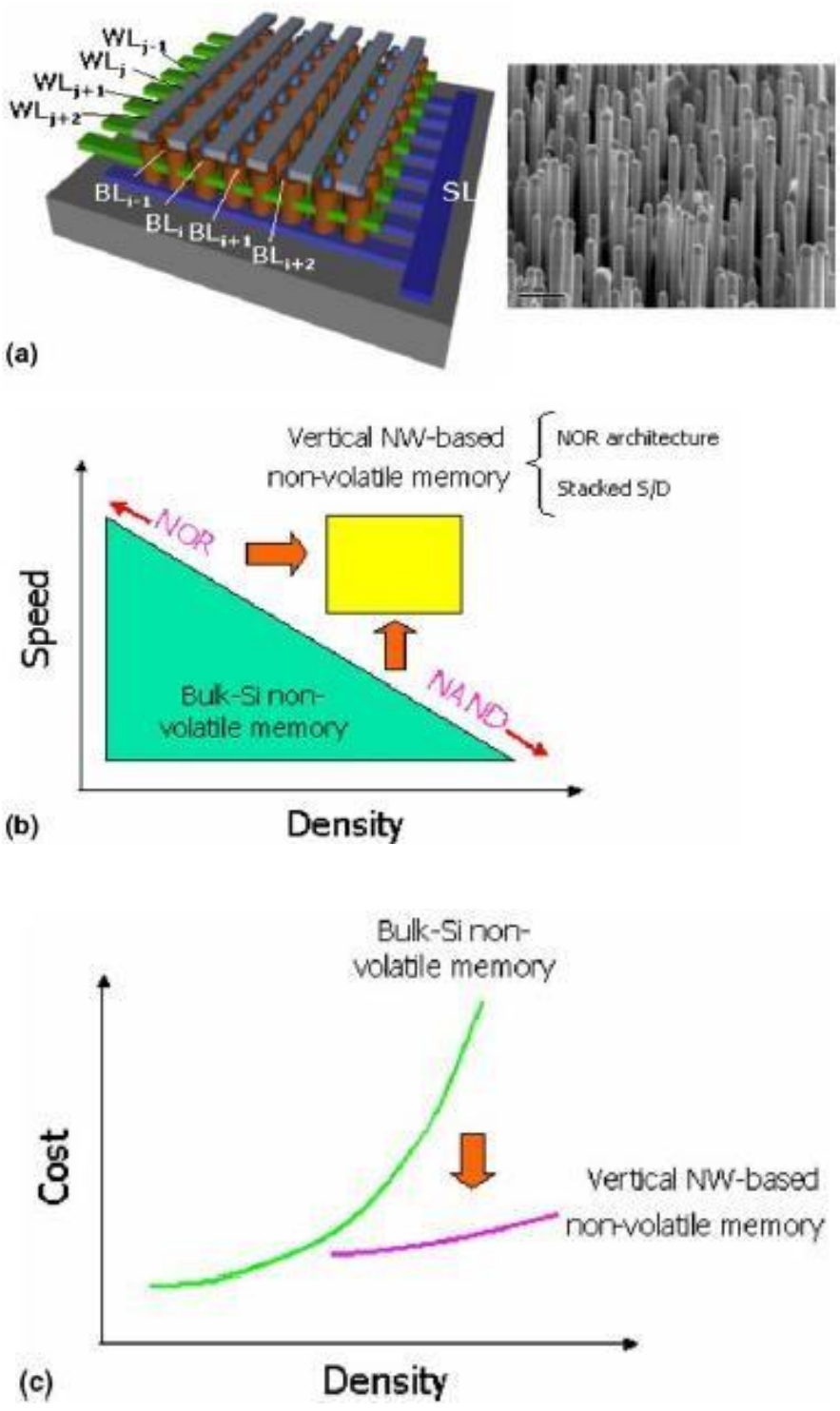

Figure 4: (a) Vertically oriented 1-D semiconductor nanowire array potentially utilized to build high-density memory chip. **(b)** Breaking the barrier of speed–density trade-off. **(c)** Cost-effectivenessof the vertical nanowire memory technology. [12]

- Crossed nanowire architecture

Crossed nanowire architecture allows a variety of electronic device elements to be built (transistors, diodes, gates etc) with a high integration density due to the tiny diameter of SiNWs. 'Crossed NWFETs can be configured from one NW as the active channel and the second crossed NW as the gate electrode separated by a thin SiO_2 dielectric shell on the SiNWsurface, with the gate on the surface of one or both of the crossed NWs [13].

The first example of the crossed nanowire architecture is the creation of a NORgate as shown in figure 5.A. It is shown that the output of the gate goes high only whenits input are both low as expected.

Another example is the implementation of a 4-bit address decoder as shown infigure 5.B.

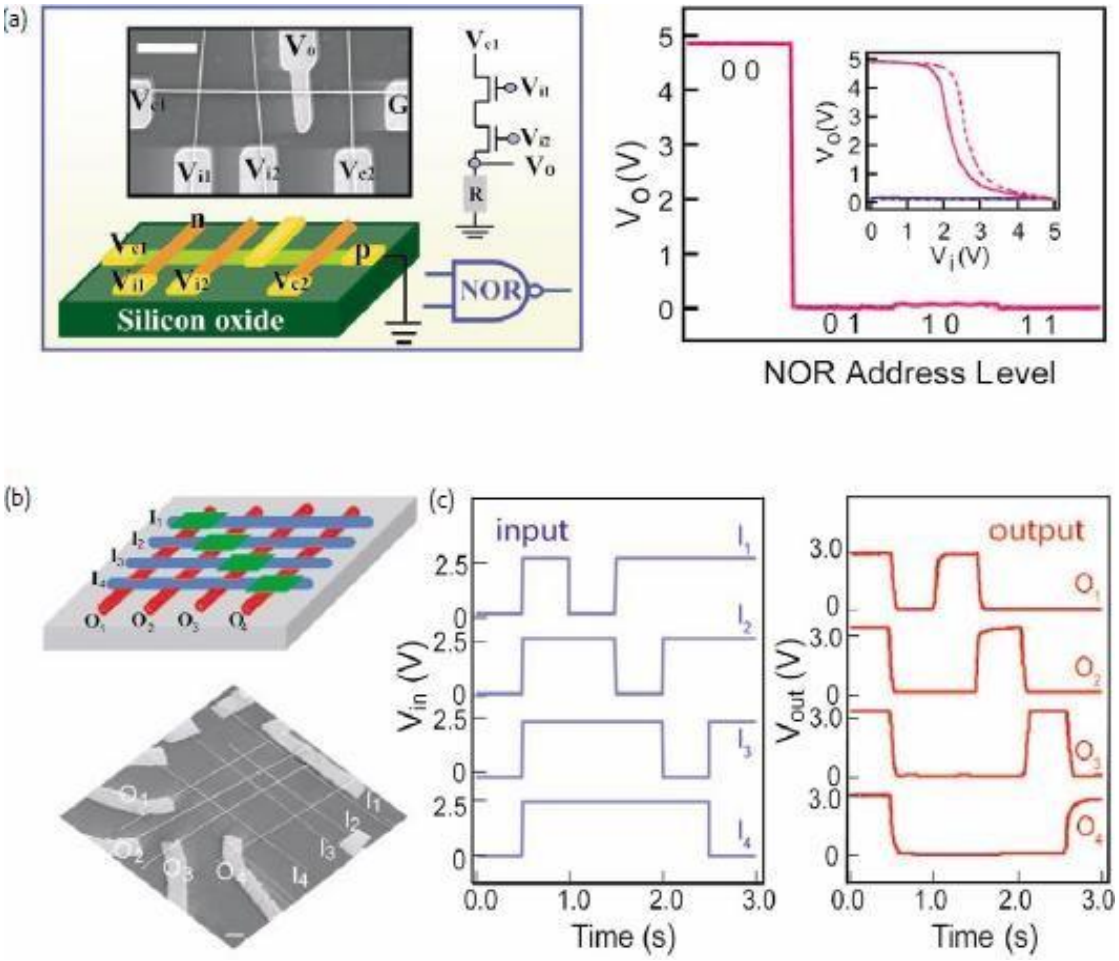

Figure 5: Crossed NW electronic devices. (left) Schematic of a logic NOR gate constructed from aone-by-three crossed NW junction array using one SiNW and three GaN NWs; insets show a representative scanning electron micrograph of the device

(scale bar, 1 μm) and symbolic electronic circuit. (right) Output voltage versus the four possible logic address level inputs; inset is the Vo-Vi relation, where the solid and dashed red (blue) lines correspond to Vo-Vi1 and Vo-Vi2 when the otherinput is 0 (1). (b) Schematic and scanning electron micrograph of a four-by-four crossed Si NW array address decoder, with four horizontal NWs (I1 to I4) as inputs and four vertical NWs (O1 to O4) as signal outputs. The four diagonal cross points in the array were chemically modified (green rectangles) to differentiate their responses from to the input gate lines. Scale bar, 1 μm. [13].

- Ring oscillator

Another experimental application of SiNW transistors is the ring oscillator (figure 6). One of its advantages over conventional fabrication methods is that the whole device integration is achieved during fabrication because of the high reproducibility of

SiNWs [13]. Also, the great stability and high performance of the SiNW ring oscillator makesit superior over the ones built with conventional planar devices [13, 14].

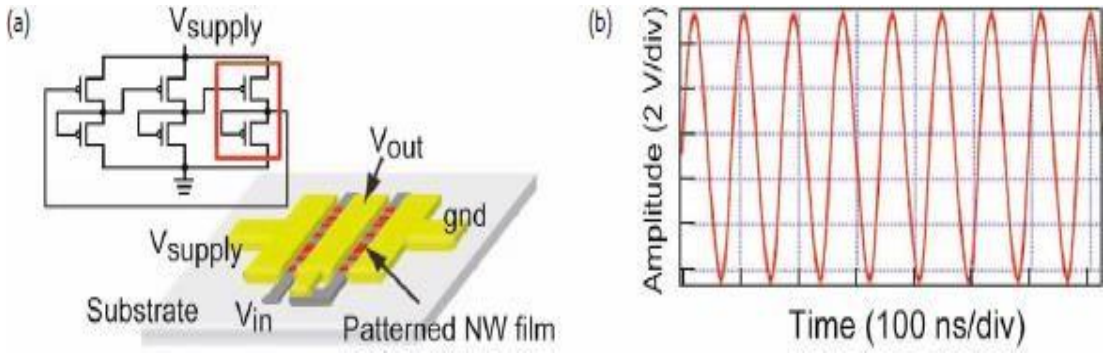

Figure 6: (a) Schematic of a multi-NW inverter on a glass substrate and a circuit diagram for a NW ring oscillator consisting of three inverters in series. **(b)** Oscillation at 11.7 MHz for a p-Si NWring oscillator with Vsupply = 43 V [13].

4. CONCLUSION

Silicon nanowires are still in an experimental stage but they can be used for the evolution of next generation nanostructures due to their extraordinaty properties compared with other nanomaterials. Their high Young's moduli and elasticity allows for the development of nano electromechanical systems (NEMS) and flexible electronics. The electrical properties of SiNWs can be well controlled during their synthesis by using the bottom-up fabrication methodand in combination with their high reproducibility SiNWs are candidates for the next generation electronics sensors.

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