

Design and Analysis of Low Power, Delay Optimized Digital Buffer Based on CNFET Technology

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Abstract

This paper presents a complete optimal design of a buffer in CMOS and CNFET 32 nm technology node. We investigate and conceptually explain the issues of power dissipation and propagation delay in CMOS and CNFET buffers driving large capacitive loads and propose a new buffer design for improving power dissipation at optimized propagation delay. The reduction in power dissipation is achieved by minimizing short circuit power and subthreshold leakage power which is predominant when supply voltage (V_{DD}) and threshold voltage (V_{th}) are scaled for low voltage applications. The proposed buffer has been designed and simulated using HSPICE tool in 32 nm VLSI technology node. The results show that modified taper buffer design provides 5-10% reduction in power dissipation at a reasonable amount of increase in propagation delay when compared with conventional design.

Index Terms— CNFET, Delay, Tapper Buffer.

INTRODUCTION

Continuous technology scaling has changed many of the problems that modern ASIC designers face in designing high performance digital circuits. With deep sub-micrometer technologies, on-chip interconnect has become a fundamental issue. High interconnect resistance and capacitance has become an important factor in limiting performance. Driving large off-chip capacitive loads is also an important design issue. High-speed Buffers are the circuit cores of many high-speed blocks within a communication transceiver. Large capacitive loads in many cases exhibit CMOS integrated circuits and tapered buffers are employed to drive these large capacitive loads at high speed, while ensuring that the load designed on previous stages of the signal path is too large. These buffers are used in the memory access path as word-

line drivers, to drive large off-chip capacitances in I/O circuits, and in clock trees to ensure that skew constraints are satisfied. But, deployment of these buffers in high-performance systems imposes a power overhead on each instance regardless to its actual performance.

High-performance VLSI design is attracting much attention because of emerging need for miniaturization, and hence design optimization for trading-off power and performance in nanometer scale integrated circuits is the need of the present scenario, which demands a decrease in both supply voltage V_{DD} (to maintain low power dissipation) and threshold voltage V_{th} (to sustain propagation delay reduction), but the fact is that the decrease in V_{th} not only increases leakage power but also short circuit power. While working in nano scale technology the total power dissipation of clock drivers, which generally have CMOS inverters, is quite large and have 30 to 50% share only of leakage current and short circuit current [1, 2].

Reduction of power dissipation in CMOS digital circuits has become an increasingly important design optimization goal. Although there are several sources of power dissipation in the CMOS technology, most of the existing power optimization and estimation techniques have focused on the dynamic power dissipation ($P_d = C_L V_{dd}^2 f$), due to the charging and discharging the load capacitances at the gate outputs. The other major source is the short circuit power dissipation (P_{sc}) which is due to the simultaneous conduction of the PMOS and NMOS transistors during the input transitions. However, as the device size and threshold voltage become smaller, P_{sc} is no longer a negligible factor. For example, for high performance circuits, if large gates are used to drive relatively small loads and if the input transition time is long, then P_{sc} becomes quite significant. [3].

To solve this problem of high power dissipation, a design scheme has been proposed, which not only minimizes short circuit power, and leakage power but also optimizes propagation delay [4, 5]. So our work presents a CMOS and CNFET taper buffer design which considers the power dissipation as dominant cost function. For better illustration and simulation purpose we are taken four stages Tapper CMOS and CNFET buffer based on that propose a modified four stage buffer design scheme.

CARBON NANOTUBE FET

Carbon Nanotube (CNT) is a sheet of graphite which is rolled up along a wrapping vector. A CNT could be single-wall (SWCNT) or multi-wall (MWCNT) [6]. SWCNTs are composed of one cylinder whereas MWCNTs have more than one cylinder. A SWCNT could be metallic or semiconducting, depending on its chirality vector, which is determined by (n_1, n_2) indices and specify the arrangement angle of the carbon atoms along the nanotube. If $n_1 - n_2 = 3k$ ($k \in Z$), the SWCNT is conducting and otherwise it is semiconducting [7, 8]. In Carbon Nanotube Field Effect Transistors (CNFETs) one or more semiconducting SWCNTs are used as the channel of the device [9] as shown in Fig. 1(a).

Types of CNFET

The first one is Schottky Barrier CNFET (SB-CNFET), which is shown in Fig. 1(b).

SB- CNFET is a tunneling device and works on the direct tunneling through a Schottky Barrier (SB) at the source-channel junction. The width of the barrier is regulated by the application of gate voltage and thus the transconductance of the device is depending upon the gate voltage. This kind of CNFET is fabricated using direct contact of the semiconducting nanotube and the metal and consequently it has a schottky barrier at the CNT-metal junction. This is highly desirable and beneficial as the interfacial barrier heights and contact transparencies of SWNT-FETs can be readily tuned by the work function of the metal S/D contacts. The main disadvantage of this technology is that the energy barrier at schottky barrier actually restricts the transconductance of the CNFET in the ON state and reduces the current delivery capability, which is a significant metric to the speed of a device. SB- CNFETs demonstrate strong ambipolar characteristics that restrict the usage of these devices in CMOS-like logic families. This type of CNFET is appropriate for moderate to high-performance applications.

To overcome the mentioned drawback of SB-CNFET, there have been attempts to develop CNFETs, which would operate like normal MOSFETs but with higher performance. Therefore, Potassium doped source and drain CNT regions have been fabricated and unipolar characteristics and the field-effect behaviour has been reached. This type of CNFET called as MOSFET-like CNFET shown in Fig. 1(c), which is operates based on the barrier height modulation by application of the gate potential. The main advantage of MOSFET-like CNFET versus SB-CNFET is that its source-channel junction has no Schottky Barrier and hence, it has significantly higher ON current. As a result, MOSFET-like CNFETs are very suitable for ultra-high-performance digital applications [10, 11 and 12]. Different kinds of CNFETs have already been presented in the literature.

Based on the mentioned advantage and disadvantage of the different types of CNFETs and also due to the similarities between MOSFET-like CNFETs and MOSFETs in terms of operation and characteristics, this type of CNFET is utilized for designing the presented circuit.

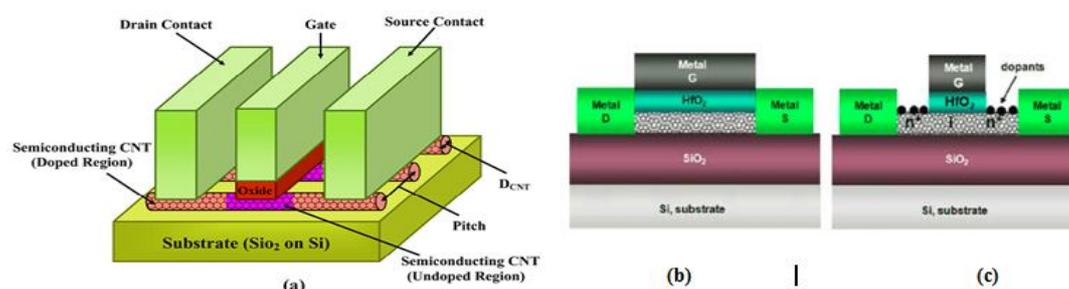


Figure 1 (a) Schematic diagram of a CNFET (b) SB-CNFET (c) MOSFET-like CNFET

Size of CNFET

Fig. 1(a) shows the schematic of a typical CNFET device. The distance between the centers of two adjoining SWCNTs under the same gate of a CNFET is called pitch,

which directly impacts the width of the gate and contacts of the device. The total size of the CNFET is determined by the width of the gate. The gate width can be determined by the pitch. By setting the minimum gate width W_{min} and the number of tubes N , the gate width can be approximated as [13].

$$W_g = \text{Max}(W_{min}, N * \text{Pitch}) \quad (1)$$

Where, W_{min} is the minimum width of the gate and N is the number of nanotubes under the gate. Moreover, the current-voltage (I-V) characteristics of the MOSFET and CNFET devices are alike.

CNFET Threshold Voltage

To design a circuit with best performance based on an average power consumption and speed, it is very important to determine the threshold voltage because this affects the switching speed, the current and leakage power. Similar to a MOSFET device, a CNFET has also threshold voltage which is the voltage required for turning on the device electrostatically through the gate. A great advantage of CNFET is that its threshold voltage can be adjusted by changing the diameter of its CNTs. This practical characteristic makes CNFET more flexible than MOSFET for designing digital circuits and makes it very suitable for designing multi-threshold circuits. The threshold voltage of a CNFET is almost considered as the half bandgap and can be calculated by the following equation [7].

$$D_{CNT} = \frac{a * \sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \quad (2)$$

where $a = 2.49 \text{ \AA}$ is the lattice constant. Since the bandgap of semiconducting CNTs is proportional to the diameter, then the threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half bandgap (which is inversely proportional to the diameter). By adjusting the diameter, the threshold voltage can be controlled and is given by [13]

$$V_{th} = \frac{E_g}{2 * e} = \frac{\sqrt{3}}{3} \frac{a * V_{\pi}}{e * D_{CNT}} = \frac{0.43}{D_{CNT} (nm)} \quad (3)$$

Where V_{π} (3.033eV) is the carbon π - π bond energy in the tight bonding model [13] and e is the unit electron charge. It can be concluded from Equation (3) that the threshold voltage of the CNFET is an inverse function of the diameter of CNT, which is calculated by the following equation (2). For instance, for a CNFET with the chiral numbers $(n_1, n_2) = (19, 0)$, D_{CNT} is 1.487nm and subsequently its threshold voltages is 0.293V.

As the chirality vector changes, the threshold voltage of the CNFET will also change. Assume that m in the chirality vector is always zero; then, the ratio of the threshold voltages of two CNFETs with different chirality vectors is given as,

$$\frac{V_{th1}}{V_{th2}} = \frac{D_{CNT2}}{D_{CNT1}} = \frac{n_2}{n_1} \quad (4)$$

From the above equation, we know that the relationship between threshold voltage and diameter of two CNFETs. For example, the threshold voltage of a CNFET using (13, 0) CNT is 0.428 V, compared to a (19, 0) CNFET with a threshold voltage of 0.293V.

PROPOSED BUFFER DESIGN

In generally the power dissipation in CMOS buffer (shown in Fig. 2.) structures is caused by charging / discharging the output load and by the short-circuit current that flows from the power supply to the ground, during switching of structures. The importance of short-circuit power dissipation in CMOS buffers, comes from the fact that a great fraction of the energy dissipated in VLSI circuits is due to on-chip and off-chip signal driver circuits, which are based on inverting buffers [14].

In addition, the problem is exacerbated when the input signal operates at high frequencies since the number of times the power dissipates in a specific interval may also be proportionately high [14, 15 and 16]. So, it is desirable to reduce the short circuit power dissipation. Hence a modified buffer is proposed [5] which dissipates less power because the short circuit component of power is eliminated in the design by tri-stating its output node momentarily before every output signal transition. This is achieved by applying the gate driving signal of PMOS (NMOS) transistor to NMOS (PMOS) transistor of the output stage through a feedback network which delays the driving signal and avoids simultaneous turn on of NMOS and PMOS transistors during signal transition which is the very cause of short circuit current.

Fig. 3 shows a 4 stage proposed taper buffer in which input signal is applied at 'Vin' which is amplified by 1st and 2nd stage. The feedback network is applied in 3rd and 4th stage, where T_1, T_4, T_5, T_7 are P-CNFET transistors and T_2, T_3, T_6, T_8 are N-CNFET transistors. INV_1 and INV_2 are minimum sized inverters which are connected to gate terminals of T_8 and T_7 for their input and with T_2 and T_5 as output respectively. The output of 2nd stage is connected to T_1, T_3, T_4 and T_6 only.

For illustration if we assume that input signal V_{in} at input terminal is at logic high level causing gate terminals of T_7 and T_8 to be at a logical low level ("logic low"). The logic low on gate terminal of T_7 is fed back through minimum sized inverter INV_2 which turns off transistor T_5 . Thus gate terminal of T_8 cannot charge until gate terminal of T_7 charges to logic high. Now, consider that input signal made a transition from a logic high level to a logic low level, transistors T_1 and T_4 turn on, and transistors T_3 and T_6 turn off. As a result, gate terminal of T_7 charges first to logic high and gate terminal of T_8 starts charging after gate terminal of T_7 is charged to logic high.

Thus, charging of gate terminal of T_8 is delayed which may cause a delay in turn on of transistor T_8 . Similarly, when input signal makes a transition from a logic low to high, gate terminal of T_8 discharges first and then gate terminal T_7 is discharged. Again, the delay in discharge of gate terminal of T_7 may cause delay in turn on of transistor T_7 . The delay in charging/discharging of gate terminals of T_7 and T_8 may avoid these transistors being on at the same time and thus reduces the short circuit power dissipation.

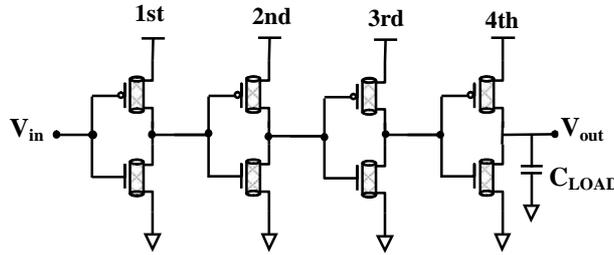


Figure 2. 4 stage Tapper Buffer

POWER AND DELAY OPTIMIZATION

In this section the optimal circuit design method for CNFET is shown. This methodology considers channel capacitance and current variations to determine the best pitch, circuit speed and area. For comparing the performance of CNFETs with MOSFETs at circuit level, the inverter as a fundamental logic gate is considered first. the inverter is designed with minimal width and a number of tubes in 32nm technology. For Si CMOS, a PMOS/NMOS ratio between 2 and 3 is used for compensating the difference in mobility between PMOS and NMOS. In this paper, a 3 to 1 (PMOS:NMOS) ratio is used when designing the inverter because the voltage transfer characteristic (VTC) of the MOSFET inverter shows a more symmetrical shape in the center of the logic threshold voltage ($V_{DD}/2$) for a ratio of 3 to 1 in 32nm CMOS technology. However for the CNFET case, a 1 to 1 (P-CNFET:N-CNFET) ratio is used because the nFET and the pFET have almost the same current driving capability with same transistor geometry [17, 18, 19]. The voltage transfer characteristics of the CNFET also has a symmetrical shape at a 1 to 1 (pFET:nFET) ratio.

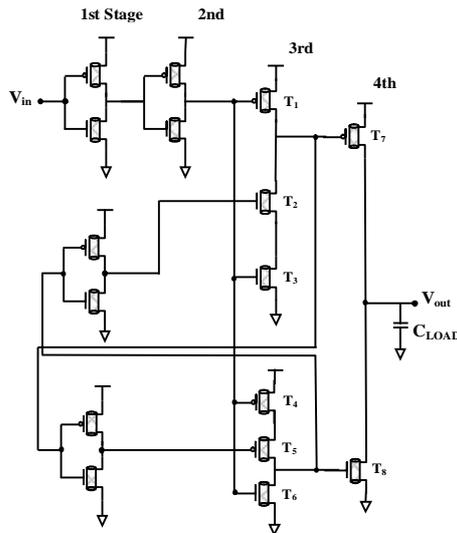


Figure 3 Proposed 4 stage modified taper buffer

In CNFET technology, the gate capacitance depends on the number of tubes and the pitch (where the pitch is defined as the distance between the centers of two adjacent CNTs in the same device [18]). As the pitch decreases, the gate capacitance is also reduced due to the potential between adjacent CNTs (affecting the total gate capacitance). Moreover, the pitch also affects the current in the CNFETs. Due to the screening effect [18], the total current of a CNFET decreases as the pitch decreases as shown in Fig. 4. By analyzing the device characteristics of a CNFET, performance metrics such as high speed, low power and low area overhead can be achieved when designing circuits using this technology.

Detailed Simulation result for the fan-out of 4 (FO4) inverter shown in Table I, the average power consumption, the propagation delay, and the PDP (Power Delay Product) for different threshold voltages are comprehensively computed.

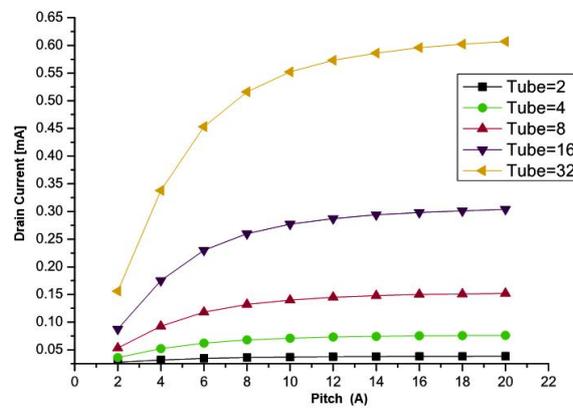


Figure 4 Drain current with different values of pitch and number of tubes.

Table II. Delay, Power and PDP of the FO4 inverter for various V_{th}

Vdd = 0.6V, Lch = 32nm, pitch = 4nm			
Diameter	2nm	1.5nm	1nm
V_{th} (V)	0.2	0.3	0.4
Delay (ns)	2.23	3.52	5.39
Power (μ W)	7.14	6.51	5.79
PDP (fJ)	15.92	22.92	31.21

The best results at each voltage are demonstrated with bold-faced numbers. When $V_{th} = 0.2V$, the smallest value of PDP is attained. Therefore in this paper, 0.2V is chosen for V_{th} . Finally we utilized this optimal parameter value for designing the proposed modified buffer circuit show in Fig. 3.

Optimization for CNFET based circuits

The optimization methods are proposed with given technology parameters. Fig. 5 shows the optimization flow overview.

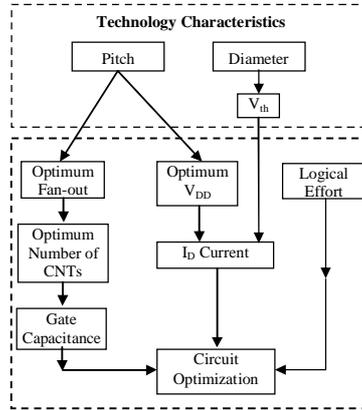


Figure 5 Optimization flow overview for CNFET based circuit.

SIMULATION RESULTS ANALYSIS AND COMPARISON

The proposed designs are comprehensively evaluated in various Load capacitance value and are compared with the other classical and state-of-the-art CMOS and CNFET-based buffer. All the designs are simulated using Synopsys HSPICE 2007 simulator tool with BSIM v4.6.1 BPTM models of MOSFET at 32nm [20] for CMOS circuits and the Compact SPICE Model [21, 22 and 23] for 32nm CNFET-based circuits, including all nonidealities. This standard model has been designed for unipolar, MOSFET-like CNFET devices, in which each transistor may have one or more CNTs. This model also considers Schottky Barrier Effects, Parasitics, including CNT, Source/Drain, and Gate resistances and capacitances and CNT Charge Screening Effects. The parameters of the CNFET model and their values, with brief descriptions, are shown in Table II.

Table II. CNFET model parameters

Parameter	Description	Value
Lch	Physical channel length	32nm
Leff	The mean free path in the intrinsic CNT Channel	100nm
Lss	The Length of doped CNT source-side extension region	32nm
Ldd	The length of doped CNT drain-side extension region	32nm
Kgate	The dielectric constant of high-k top gate dielectric material	16
Tox	The thickness of high-k top gate dielectric material	4nm
Csub	The coupling capacitance between the channel region and the substrate	20pF/m
Efi	The Fermi level of the doped S/D tube	6eV

Due to the increased demand for high-speed, high-throughput computation, and complex functionality in mobile environments, reduction of delay and power

consumption is very challenging. MOSFET and CNFET can be compared using the Power and Delay as metric. The results are summarized in table III compare propagation delay and power dissipation for the proposed and conventional buffer circuits in 32nm MOSFET and 32nm CNFET technologies.

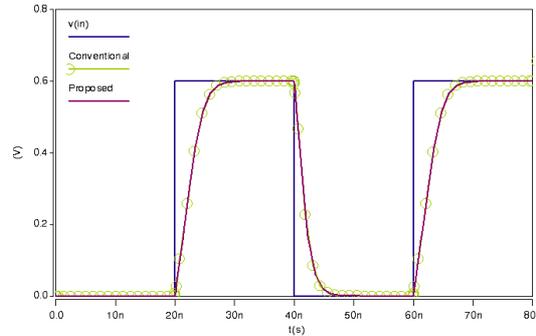


Figure 6 Simulation result of the 4 Stage conventional and proposed CNFET buffer Circuit at load $C_L=150\text{fF}$

The results in table III which shows a comparison result of state art of the 32nm CMOS and CNFET technology. From the simulation result, CNFET technology based buffer circuit have a low propagation and low power dissipation as compare to CMOS technology. In CNFET technology, an increase in propagation delay of around 0.7% and decrease in power dissipation of around 10% in the proposed design as compared to conventional design. This is because of the presence of feedback network which, uses more number of transistors as compared to conventional design, causes a small increase in propagation delay. Comparison shows that when load capacitance $C_L=1500\text{fF}$, power dissipation reduction in this case is more which is about 14% at the cost of increase in delay of about 3-4%. The result table also shows that the comparison between CMOS and CNFET 32nm technology performance variation in terms of power and delay. The simulation results demonstrate that the proposed circuits are superior in terms of speed, power consumption with respect to conventional buffer designs.

LAYOUT

Electric is a very powerful CAD system for custom design of integrated circuits (ICs). The tool supports CNFET schematic and layout entry, rule checking, and HSpice / Verilog A netlist generation. It provides users with a customizable CNFET technology library with the ability to specify λ based design rules. Fig 7 and 8 shows a screenshot of conventional and proposed buffer circuit layout panel. The layout is created using ‘mocmos-cn’ technology [24] (“cn” = carbon nanotubes).

Electric provides three rule checking tools to validate circuit layouts. In order to verify that a schematic and layout are equivalent, LVS is performed. This tool ensures that circuit topologies, transistor sizes, and input/output pins match exactly.

Then, electrical rule checking (ERC) is performed. This tool determines whether there are substrate contacts in every area of a p-/n-well region. A p-/n-well substrate contact is connected to GND/VDD, respectively, to prevent latchup problem in CNFET technology.

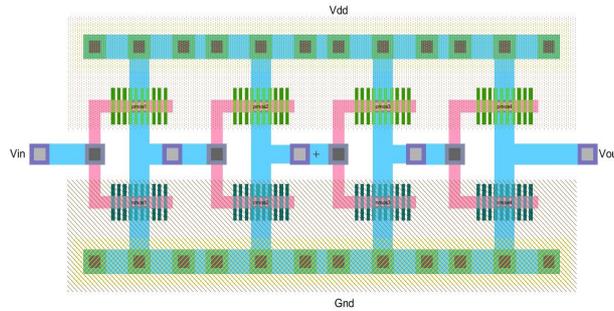


Figure 7. 4 stage Tapper Buffer

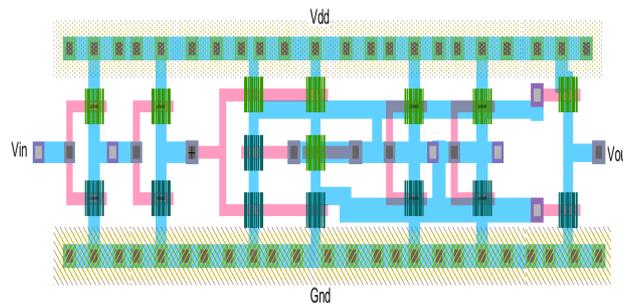


Figure 8. Proposed 4 stages modified Taper Buffer

Table III. Simulation and Comparasion result of Conventional Buffer design and Proposed Buffer design

Load Capacitor C_L (fF)	Parameter	32nm BSIM CMOS Model		32nm CNFET Model		% increase in propagation delay		% decrease in power dissipation	
		Tapper Buffer	Proposed Buffer	Tapper Buffer	Proposed Buffer	32nm BSIM CMOS	32nm CNFET Model	32nm BSIM CMOS	32nm CNFET Model
15	Propagation delay (ns)	0.981	0.989	0.746	0.750	0.8	0.4	-	-
	Power dissipation (μ W)	0.3437	0.2895	0.3463	0.294	-	-	5.42	5.23
150	Propagation Delay (ns)	2.632	2.647	2.402	2.409	1.5	0.7	-	-
	Power dissipation (μ W)	3.6205	3.5005	1.1498	1.0468	-	-	12	10.30

1500	Propagation Delay (ns)	3.259	3.306	2.769	2.801	4.7	3.2	-	-
	Power dissipation (μ W)	5.2004	5.0104	4.8921	4.7449	-	-	19	14.72

CONCLUSION

In this paper, power dissipation and propagation delay parameters have been optimized during design of CNFET buffer driving large capacitive loads. The paper makes it possible to quantitatively estimate the delay, and power of digital buffer circuit. This has been accomplished by proposing an optimization methodology for CNFETs. As the characteristics of a CNFET is different from conventional bulk CMOS, new criteria must be established. By an appropriate selection of the diameter from the chirality, threshold voltages are determined. As the channel capacitance and current vary as pitch is changed due to the screening effect, the gate capacitance has been established as function of the number of tubes in the device and the optimum fan-out factor has been found. Using this parameter, the logical effort has been calculated and the minimum delay of a multistage circuit topology has been analysed. To prove the effectiveness of the proposed gate-level design method, simulation has been performed using HSPICE with the CNFET library of [23], To design a CNFET circuit, many parameters must be considered, among them the diameter at certain chirality, pitch and the optimum number of tubes have been shown to be of primary importance. Comprehensive simulations, analysis and comparisons demonstrate the superiority of the proposed structures in terms of speed, power consumption. An improvement of 5-10% in power dissipation has been achieved at a reasonable amount of increase in delay as compared to the existing design. Hence, the proposed buffer can be used to provide power efficient solutions for portable VLSI applications at optimum propagation delay.

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