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# Low Power Design of 8 Bit Adder in MTCMOS Circuit Using Tri Mode Technique

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## ABSTRACT

Multi-threshold CMOS (MTCMOS) is a variation of CMOS chip technology which has transistors with multiple threshold voltages in order to optimize power or delay, which is also known as power/ground gating is the most commonly used leakage power suppression technique in state-of-the-art ICs. Input transition noise is the most important reliability issue in MTCMOS circuits. Wake up (sleep) signal slew rate modulation is an alternative technique that is effective for suppressing the ground bounce noise in MTCMOS circuits. A tri-mode multi threshold CMOS technique is proposed in this paper. With the new digital tri-mode MTCMOS technique, fast and energy efficient mode transitions are achieved with negligible ground bounce noise in MTCMOS circuits. The simulation results are characterization of 120nm CMOS technology using DSCH and MICROWIND tools.

**KEYWORDS:** MTCMOS circuit technique, Brent Kung adder, tri-mode MTCMOS technique.

## INTRODUCTION

A common implementation of MTCMOS for reducing power makes use of sleep transistors. In multi threshold CMOS there are two threshold voltages that is Low threshold voltage and High threshold voltage [1]. Low threshold voltage cells (8 bit adder) are used in the logic where fast switching speed is important where as High threshold voltage cells (sleep transistors) are used where leakage has to be prevented. MTCMOS logic is effective standby leakage circuit technique, but it is difficult to

implement, So that sleep transistor sizing is highly dependent on discharge pattern within the logic block. They showed dual threshold voltage (Vth) domino logic avoids the sizing difficulties and inherent performance associated with MTCMOS. Both the transistors or cells are effectively used in MTCMOS technique.

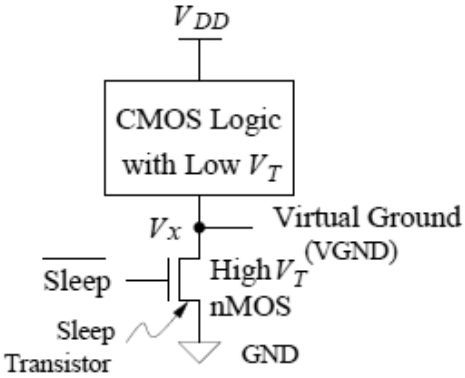


**Fig 1:** MTCMOS circuit structure

In the active state of operation the high threshold voltage transistors are turned ON and the logic gates consisting of low threshold voltage transistors can operate with low switching power dissipation and smaller propagation delay.

In the standby state of operation the high threshold voltage transistors are turned OFF thereby cutting off the internal low threshold voltage circuitry. Multiple threshold voltage CMOS technique is used the both Low and High threshold voltage transistors [2] _ [8]. Use low threshold gates on critical path while higher threshold gates off the critical path. This methodology improves speed without an increase in power. The design of the power switch which turns ON and OFF the power supply to the logic gate is essential to low voltage, high speed or performance circuit techniques such as MTCMOS. The speed, area, and power of a circuit are influenced by the characteristics of the power switch [3].

## 2. TRIPLE-PHASE SLEEP SIGNAL SLEW RATE MODULATION TECHNIQUE

The triple-phase sleep signal slew rate modulation technique is used to reduce power and ground bounce noise in Multi threshold CMOS circuits. The wake up (sleep) signal is raised from 0 V to the threshold voltage of sleep transistor in order to optimize the overall reactivation time without producing significant noise. Ground bounce noise is primarily produced after the sleep transistor is turned ON. The wake up (sleep) signal should be therefore subsequently decrease the gate voltage level reaches the threshold voltage of sleep transistor. Decrease of wake up signal, suppresses the peak ground bounce noise that is produced after the sleep transistor is fully activated. After the Virtual ground voltage is reduced to a very low level close to 0 V, the input transition noise is negligibly low level. The rise of wake up (sleep) signal should therefore be again accelerated to shorten the remaining duration of reactivation process. Due to this Phase 1 and Phase 3, the reactivation time and energy

consumption of multi threshold CMOS circuits are reduced with the triple phase sleep signal slew rate modulation technique [5].

The triple phase sleep signal modulator with 1 bit adder is shown in the Fig.2, the rising speed of wake up signal is adjusted by monitoring the voltage level of input of the sleep transistor and virtual ground. The sleep global is the input signal of the triple phase which is shown in the Fig. 2. Sleep local is applied to the gate terminal of the sleep transistor which is shown in the fig. that controls the ground connection of a circuit block. With the triple phase sleep signal slew rate modulator that is shown in Fig. 2, the rising speed of sleep signal is adjusted by monitoring the voltage level of sleep local and virtual ground. The transitions between the three phases of reactivation occur automatically.

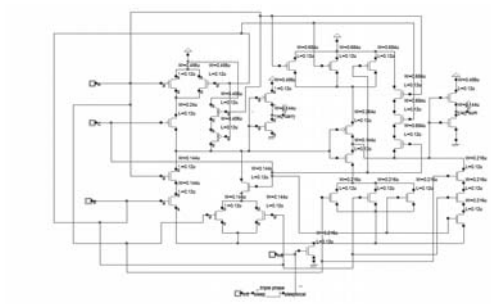

**Fig 2:** Triple Phase using sleep transistor with 1bit adder Circuit Diagram

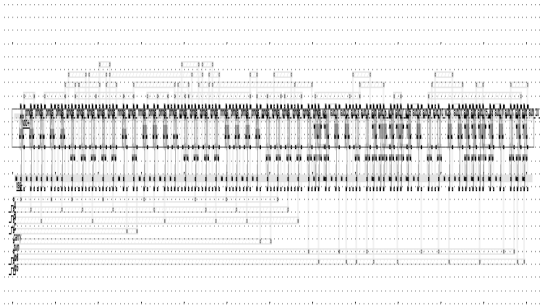

**Fig 3:** Layout for Triple Phase using sleep transistor with 1bit adder Circuit Diagram

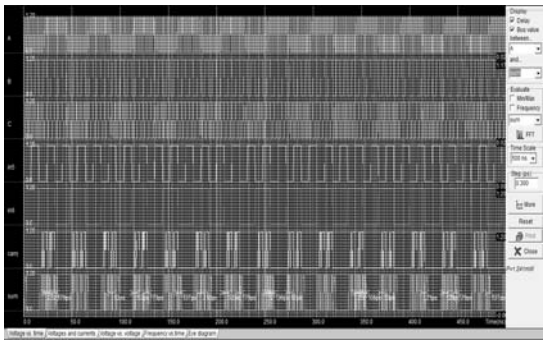

**Fig 4:** Power Estimation for Triple Phase

## 3. TRI-MODE MTCMOS TECHNIQUE

The proposed tri-mode MTCMOS technique is presented in this section. An Additional intermediate PARK state is introduced between SLEEP and ACTIVE states to reduce the power and ground bounce noise that is produced during reactivation events. A High threshold voltage PMOS transistor (Parker) is connected in parallel with the sleep transistor (Footer) as illustrated In Fig5.

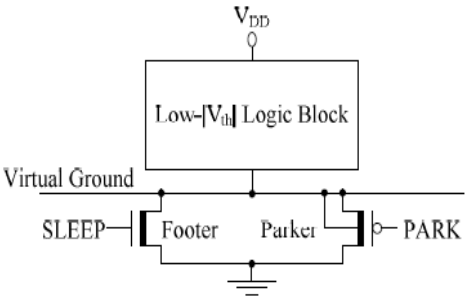


**Fig 5:** Basic Tri Mode Circuit Diagram

The Low threshold voltage logic block consisting of the 8 bit adder is shown in the Fig6 and Fig9. When a tri mode MTCMOS circuit is in sleep mode, the sleep transistors footer and parker are in OFF state to place the circuit in to low leakage sleep mode as shown in the Fig9. During sleep or standby mode, the virtual ground line is approximately the power supply voltage. The effective supply voltage that is completely crushed to approximately 0v in Multi threshold CMOS circuit. The subthreshold current is produced by the low threshold voltage logic block are there by reduced in sleep mode.

At the end of an idle period, the parker is turned ON while the footer is OFF as shown in Fig8. The activation of the circuit transitions to the intermadiate park mode. The virtual ground line is discharged to the threshold voltage of the parker. The first wave of output is produced by the transition from sleep mode to the park mode.

Subseqently, in activation process the footer is turn ON to discharge the Virtual ground line to 0v as shown in Fig11. During this transistion the second wave of output is produced. In the active mode, the effective supply voltage of low threshold voltage circuit block is equal to the power supply voltage VDD. Thatswhy the tri mode MTCMOS circuit is high performance in active mode of operation. The power and ground bounce noise can be reduced by adjusting the size of the parker in a tri mode technique.

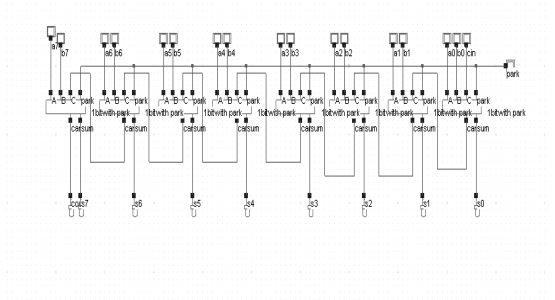

**Fig 6:** Tri mode technique with park signal

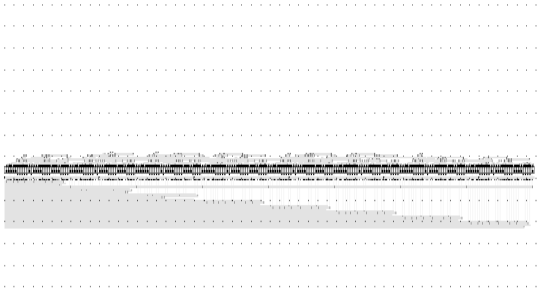

**Fig 7:** Layout for Tri mode technique using 8bit adder Diagram with park signal

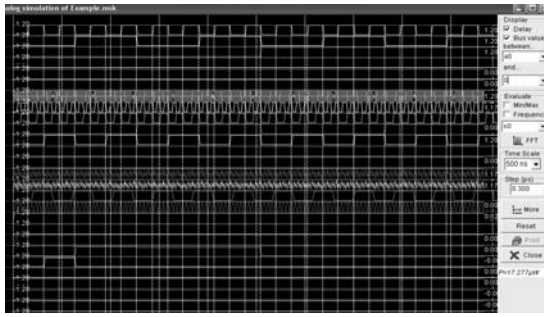

**Fig 8:** Tri Mode Operation When Sleeep Is OFF and Park Is ON.

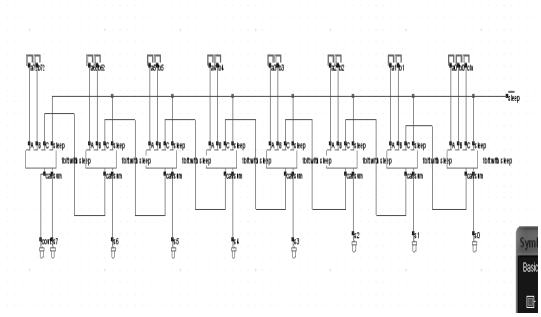

**Fig 9:** Tri mode technique with sleep signal

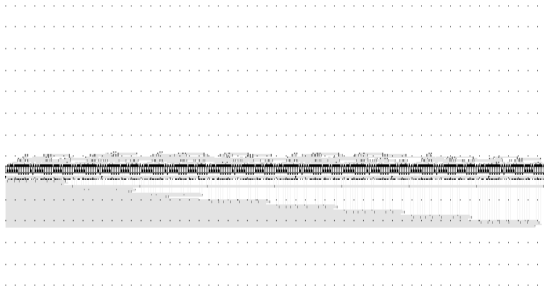

**Fig 10:** Layout for Tri mode technique using 8bit adder Circuit Diagram with sleep signal

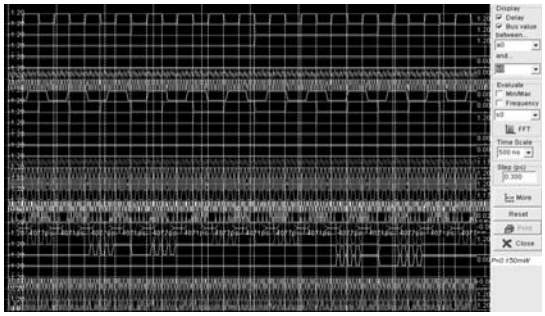

**Fig 11:** Tri Mode Operation When Sleep Is ON And Park Is OFF.

## 4. COMPARISON OF RESULTS

**TABLE 1**

| Parameter | Exiting system | Proposed system |
|---|---|---|
| Power | 1.241mw | 1. Sleep off and park on; p=92.382uw<br>2. sleep on and park off; p=0.150mw |
| Leakage current | 110nA | 91.8nA |
| Layout area | 888um2 | 7056um2 |

In this paper final result the Power is reduced to 92.382uw when sleep is OFF and park is ON where as 0.150mw when sleep is ON and park is OFF. The another parameter leakage current is also reduced to 91.8na which is shown in the above figure and layout area is increased.

## 5. CONCLUSION

Wake up (sleep) signal slew rate modulation techniques are explored in this paper for reducing input transition noise in MTCMOS circuits. A triple phase technique using

sleep transistor is presented and tri mode technique is proposed. Comparing both the techniques that is triple phase and tri mode, tri mode circuit shows the lower delay and power when compared to triple phase.

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