

Design of MIMO OFDM SDM Systems for High Speed Data Transmission

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ABSTRACT

A combination of Multiple-Input Multiple-Output Spatial Division Multiplexing technology and Orthogonal Frequency Division Multiplexing technique, namely MIMO-OFDM SDM systems, been well-known as a potential technology to provide high speed data transmission and spectrum efficiency for modern wireless communications networks. The rising development of Internet related contents and demand of multimedia services leads to increasing curiosity to high speed communications. It has been shown that by using MIMO system architecture, it is possible to increase that capacity considerably. The combination of MIMO-OFDM is beneficial since OFDM enables support of more antennas and larger bandwidths since it simplifies equalization in MIMO systems. Moreover fading is considered as a problem in wireless communication but MIMO channels uses the fading to increase the capacity of entire system.

The paper proposes the design of MIMO OFDM SDM system includes transmit side, MIMO channel, and receive side. The process of design consists of Matlab Simulation and Verilog HDL Design. The system performance is evaluated based on bit error rate (BER) criteria, and the efficiency of design also can be done through the calculation of the FPGA element consumption.

Index Terms: - MIMO OFDM, SDM System, BER, FPGA

INTRODUCTION

A combination of Multiple-Input Multiple-Output Spatial Division Multiplexing technology (MIMO SDM) and Orthogonal Frequency Division Multiplexing (OFDM) technique has been considered as a potential technology for high speed data wireless transmission networks, such as IEEE 802.11, 3GPP Long Term Evolution, and WiMAX [1-5]. The MIMO SDM technology can significantly increase channel

capacity by simultaneously transmitting multiple independent substreams with the same data rate and power level. Meanwhile, the OFDM technology can eliminate the effect of multipath fading and use given spectrum efficiently.

In [9], authors presented the design and implementation results of a digital 120 Mb/s MIMO orthogonal frequency division multiplexing (OFDM) wireless LAN (WLAN) baseband processor based on the proposed decoding algorithms. In [10], a prototype field programmable gate array (FPGA) implementation of an OFDM physical layer is shown using the Xilinx System Generator. In [11], authors presented an experimental broadband wireless 4x4 MIMO-OFDM system operating at two well-known WLAN frequency bands: 2.4GHz and 5.2GHz. Designer described by placing special emphasis, both at the radio frequency and digital signal processing levels, on the design of reconfigurable hardware architecture. In these papers they have not considered the consumption of FPGA elements in their system design, which evaluate the efficiency of system design. In addition, a detailed design and implementation of the MIMO-OFDM systems have not fully described.

The main contribution of the paper is to present design and implementation of the systems on the FPGA-based DSP Kit. A detailed design of full systems included transmit side, MIMO channel, and receive side is shown. The system performance is evaluated based on biterror rate (BER) criteria, and the efficiency of the design is shown through the calculation of the FPGA element consumption. This paper is divided into five parts as follows. After a brief introduction, an overview of MIMO-OFDM SDM systems is described in section II. In section III, present the design and hardware implementation of the viterbi decoder in MIMO-OFDM SDM systems. The simulations are shown in section IV.

II. MIMO-OFDM SDM SYSTEMS

Figure 1 shows the basic MIMO SDM NR x NT system. Let H denote as a channel matrix. The transmitted spatially multiplexed data and the corresponding received signal are presented by $x = [x_1, x_2, \dots, x_{NT}]^T$, $y = [y_1, y_2, \dots, y_{NR}]^T$ respectively. The received signal can be written by

$$Y = Hx + z \quad (1)$$

where $z = [z_1, z_2, \dots, z_{NR}]^T$ is the white Gaussian noise, in which each z_i is an independent Gaussian process with zero mean and variance σ^2 , H is MIMO channel matrix described as below:

$$H = \begin{pmatrix} h_{11} & h_{12} & \cdots & h_{1N_{TX}} \\ h_{21} & h_{22} & \cdots & h_{2N_{TX}} \\ \vdots & \vdots & h_{ij} & \vdots \\ h_{N_{RX}1} & h_{N_{RX}2} & \cdots & h_{N_{RX}N_{TX}} \end{pmatrix}, \quad (2)$$

Where h_{ij} is the channel response from the j^{th} transmit antenna to the i^{th} receive antenna

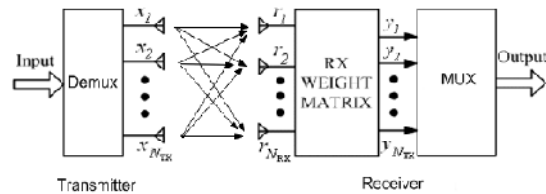


Fig. 1. Block diagram of MIMO SDM system

To detect received signals, a receive weight matrix is used to detect the received signals.

Fig. 2 shows a block diagram of MIMO-OFDM SDM systems. On each transmit antenna, the complex data stream is done by IFFT process, and then adds cyclic prefix signals to mitigate multipath effects. At the receive side, received signals are first removed cyclic prefix signals, and then converted to frequency domain by FFT process. Signals on each subcarrier are then detected by a receive weight matrix to obtain transmitted data.

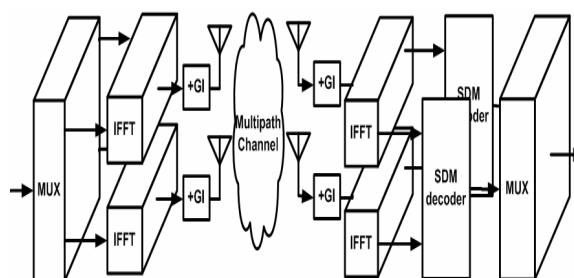


Fig. 2. Block diagram of MIMO-OFDM SDM system

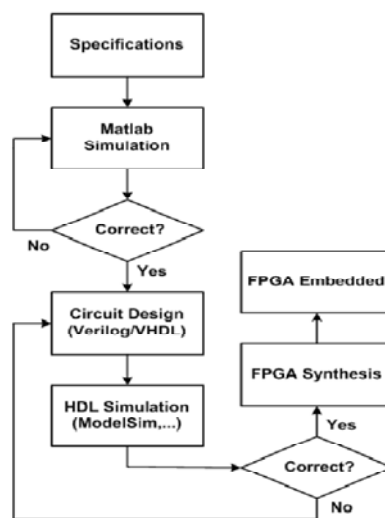


Fig. 3 Design process

MATLAB SIMULATION:-

The design of a simulation system on Matlab Simulink is absolutely necessary before start to design system with Verilog HDL. It not only provides the results to compare, but also is the foundation on which can set the required parameters as well as easily debug errors for hardware model.

Figure 4 shows: a design of 2x2 MIMO-OFDM SDM systems on Matlab Simulink. It includes block: modulation, demodulation, add-training symbol, FFT/IFFT.channel estimation and SDM decoder.

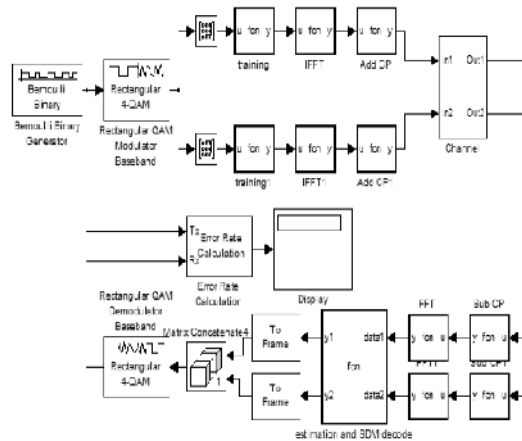


Fig. 4. Matlab Simulink simulation system

The hardware receiver description is shown in Fig. 5. It mainly includes 4 processing block: OFDM demodulation, channel estimation, ZF (zero forcing) decoder, and digital demodulation. At the receiver, the channel coefficients $h_{i,j}$ are estimated by using preamble training sequences which were created at the transmitter. The channel coefficients after that are used for extracting data.

Detector modules of MIMO-SDM systems are placed after estimation module. By performing ZF algorithm detection can take the complex data streams back.

At the receiver, the complex data streams are demodulated by “4QAM demodulation module”. After that, compare the received bit stream to the transmitted bit stream to calculate BER performance of the systems

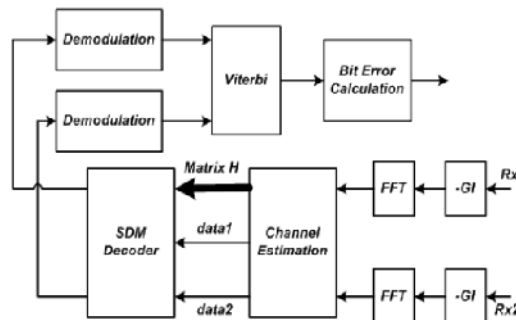


Fig. 5 Receiver

III VERILOG HDL DESIGN

The system design with Verilog HDL has disadvantages such as long design time, difficult simulation and error in debugging. It also requires the designer to master the theory and have good experience in their subject. To overcome this, we can design system by switching from C to HDL language or the use of IP core already completed. However, both methods have two common drawbacks. First one, it's taking a very high cost to purchase licensed programs or get the ownership of the IP core. Second, it's not high academic

Therefore, considering the advantages of the design in Verilog, reducing costs to a minimum while being highly academic. The objective is to design the viterbi decoder section of MIMO-OFDM SDM systems on FPGA .

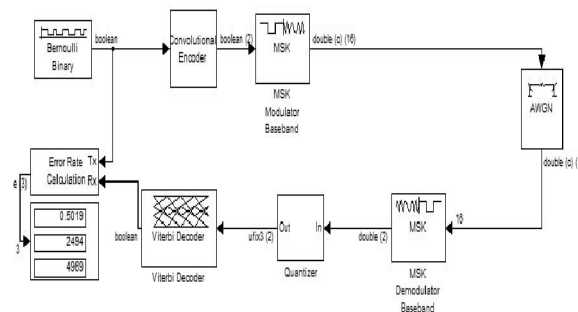


Fig. 6 simulink block for viterbi decoder

IV SIMULATION RESULTS:-

BER performance for mimo ofdm sdm systems with different modulation schemes such as BPSK, QPSK and QAM

Table 1. BER and SNR calculations

MODULATION	BER	SNR(dB)
BPSK	0.5008	11.82
QPSK	0.5007	17.36
16-QAM	0.5003	17.44
64-QAM	0.489	18.23

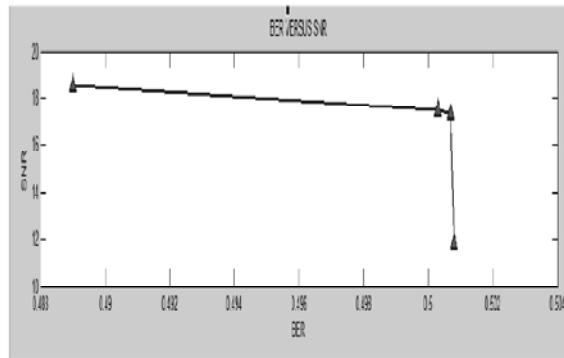


Fig. 7 BER versus SNR

In above figure reveals that the BER rate is decreased as the order of modulation increases. In BPSK the BER rate is high when compared with QPSK and QAM. Signal-to-noise ratio is defined as the power ratio between a signal (meaningful information) and the background noise (unwanted signal). Also SNR is high for highest order of modulation. It is possible to enhance the SNR by averaging the measurement when the signal is constant or periodic and the noise is random. The noise will go down as the square root of the number of averaged samples in this case.

HDL CONVERSION

From MATLAB functions, Simulink models, and State flow charts, HDL Coder generates portable, synthesizable Verilog and VHDL code. The generated HDL code can be used for FPGA programming or ASIC prototyping and design. The HDL Coder will provide a workflow advisor that automates the programming of Xilinx and Altera FPGAs.

The Viterbi Decoder block decodes input symbols to produce binary output symbols. This block can process several symbols at a time for faster performance. This block can output sequences that vary in length during simulation.

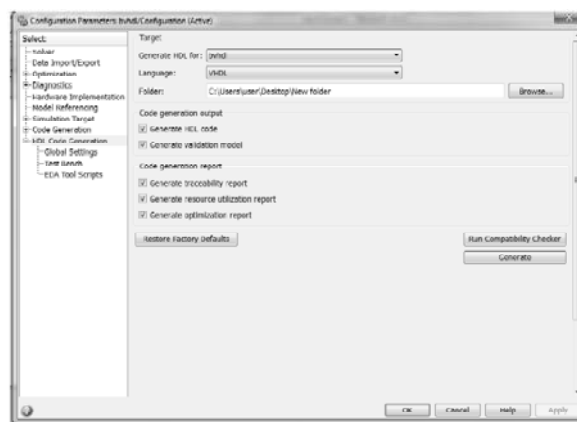


Fig. 8 HDL Conversion window
Table 2. Device utilization report

MODULATION	M-PAM	MSK
NO: OF OCCUPIED SLICES	3562	3993
NO: OF 4 INPUT LUTS	4286	4390
NO: OF SLICE FLIPFLOPS	3907	4419
REGISTERS	3352	3416
ADDERS/SUBTRACTORS	141	142
MULTIPLEXERS	330	356

V CONCLUSION

MIMO-OFDM SDM technology has been considered a candidate for high speed wireless data transmission networks because of its significant increase of channel capacity and use of spectrum efficiently. Based on the design, measured and evaluated BER and SNR performance of the systems. Hence QAM has better performance than other modulation schemes such as BPSK and QPSK in terms of BER and SNR. Here, also considered the consumption of elements for a viterbi decoder by HDL conversion. It has shown the efficiency of the design. As the complexity of modulation increases, the area utilization also increases.

This work is devoted to space-time coding for multiple- input/multiple-output (MIMO) systems. The concept of space-time coding is explained in a systematic way. Alamouti code is the only OSTBC that provides full diversity at full data rate (1 symbol/time slot) for two transmit antennas.

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