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Quadrature Oscillator: A New Simple Configuration based on 45nm 2nd Generation CMOS Current Controlled Current Conveyor

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Abstract

Quadrature oscillator is an important building block used in various applications of signal processing and communication. Here a new and simple scheme is presented for quadrature oscillator realization using two second generation current controlled current conveyors (CCCII+ and CCCII-). This circuit scheme uses only two grounded capacitors and is also resistor free. The CCCII's are designed in 45nm CMOS technology and posses the advantages of current mode techniques.

Keywords: Current conveyor circuits; Current controlled current conveyor circuits(CCCII);Quadrature oscillator

Introduction

At present there is a growing interest in using current conveyors for designing analog signal processing circuits. The current mode (CM) techniques are attributed to the larger bandwidths and wider dynamic ranges obtainable compared to the classical operational amplifier based circuits. Basically a CCCII is four terminal device which can be used with the other electronics elements in specific circuit configurations, can perform many useful analog signal processing functions [1,4].A current conveyor is said to be capable of simplifying the circuit design in much the same manner as the conventional operational amplifier along with the added advantages of current mode approach. The current conveyor was originally conceived by Smith and Sedra who presented the first generation conveyor and subsequently the second generation conveyor [2].

Current conveyor (CCII) has attracted the attention of designers in the field of active filters and oscillators due to its distinct advantages over operational amplifier. This is attributed to their larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry and low power dissipation [1, 4]. By the advent of second generation current controlled current conveyor (CCCII) [4,8], the applications of current conveyor have been extended to the domain of electronically adjustable functions. Electronic adjustability of CCCII is attributed to the dependence of resistance at port X on the bias current. In effect, a CCCII is found capable of replacing a CCII and a resistor thereby simplifying the design process and the hardware requirement of the design. Hence in publications of the recent past, the designers have put great emphasis on the design of oscillator circuits using CCCII [9, 10].

In the recently published literature, a number of schemes can be found to realize current conveyor based oscillators [2-7]. These schemes, invariably, are based on two or more CCII's/CCCII's, along with many resistors and capacitors.

The purpose of this paper is to propose a novel quadrature oscillator structure employing two CCCIIs, one being a positive CCCII and the other one a negative CCCII and only two grounded capacitors . The resulting structure offers electronic tunability of frequency of sinusoidal oscillation and other usual advantages of the current mode techniques.

Electrical characteristics of CCCII

The electrical characteristics of CCCII$\pm$ can be summarized as follows:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_X & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

Where the + and – signs in the third row and second column express the type of the CCCII. In case of a CCCII-, the direction of I_X or I_Z is reversed as compared to the directions for the CCCII+, i.e. $I_Z = -I_X$ in case of CCCII-.The block diagram given below shows a CCCII+

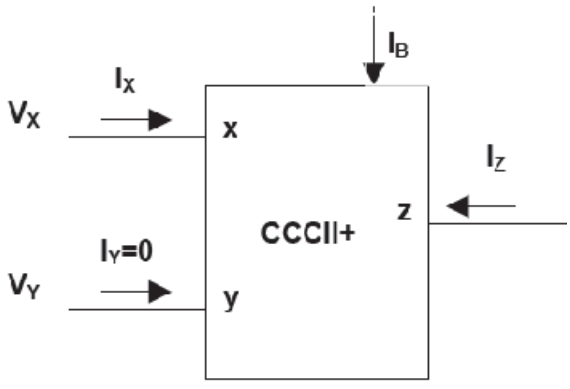

Figure 1: Block Diagram representation of the 2nd generation CCCII+.

Proposed Quadrature Oscillator Configuration

A Quadrature oscillator is an special class of phase shift oscillators which produces sinusoidal oscillations and it's corresponding 90^o phase shifted output simultaneously. Thus if $V_3(t) = A\,cos\omega t$ then

$$V_4(t) = \text{Acos}(\omega\text{t} \pm 90^0) = \mp A sin(\omega t)$$

The signals $V_3(t)$ and $V_4(t)$ can also be expressed as differentials of one another.

Thus $V_4\,(t) = -Asin(\omega t) = \frac{d}{dt}\,A\cos\,(\omega t)$ .This equation can be expressed in Laplace transform as

$$V_4\,(s) = s\,V_3(t)$$ [8].

In Figure 2 below, a novel circuit scheme is proposed which realizes a current mode quadrature oscillator. This circuit enjoys the circuit simplicity, as it utilizes a CCCII+, a CCCII- and just two capacitors. A CCCII- is different from a CCCII+ only in its output stage; otherwise, their principle architecture remains the same. Therefore, the values of their parasitic resistances are assumed equal [4].

For performing routine analysis, node equations can be written on nodes (3) and (4) of figure 2

$$V_3(s).sCR = V_4 \quad (2)$$

$$V_4(s).sCR = V_3 \quad (3)$$

Solving the above equations we obtain the following characteristic equations.

$$s^2C_1C_2R_{X1}R_{X2} = -1\ (s = j\omega\,, s^2 = -\,\omega^2) \quad (4)$$

$$\omega^2C_1C_2R_{X1}R_{X2} = 1 \quad (5)$$

Applying the choice of equal components, $C_1 = C_2 = C_P$; $R_{X1} = R_{X2} = R$, the frequency of oscillations is simplified to

$$\omega = (CR)^{-1} \quad (6)$$

Again considering the equations (2) and (3) , it can be seen that the node voltages V_3 and V_4 are quadrature voltages of one another.

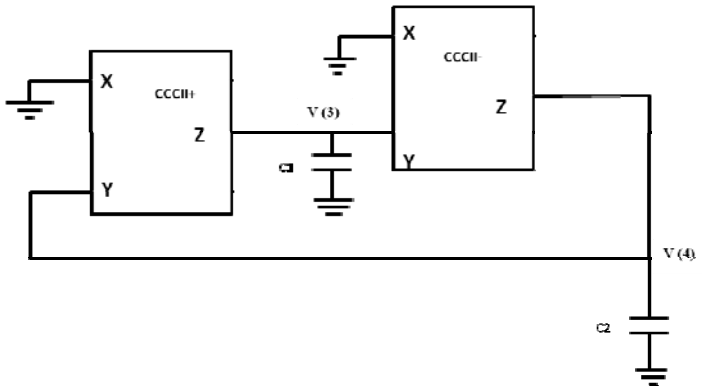

Figure 2: Block diagram of Quadrature Oscillator using CCCII±

For realizations, of the above Quadrature oscillator, 45nm CMOS design of CCCII is adopted from [4], and the oscillator of figure 2 is simulated on HSPICE using PTM 45nm CMOS parameters from Berkeley. The simulation results of the quadrature oscillator are presented in figure 3 and figure 4. Figure 3 shows the oscillations generated by the oscillator at node 3 whereas, figure 4 shows the oscillations at node 3 and 4 indicating the phase shift of signal of node 4 with respect to node 3.

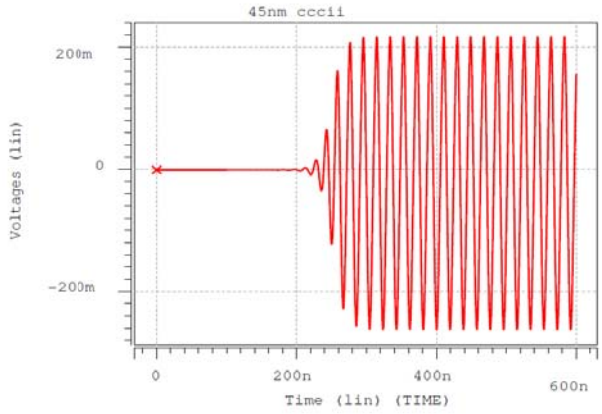

Figure 3: Output of the proposed oscillator (node 3). I_B=2µA , C=1pF, oscillation startup time 170ns

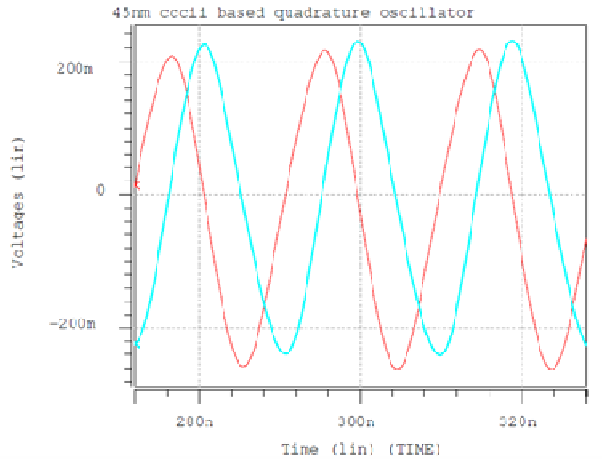

Figure 4: Expanded view of the output signal at node (3) and (4) of the fig.3

From figure 4, the time period of the oscillations is 19.14ns. Further the phase difference of the signal at node 3 and 4 is calculated by observing the adjoining zero crossovers of two signals, (and transforming them into the equivalent phase difference of 89.81^0.

Verification and Results

The graph shown below in figure 5(a) is plotted across the frequency of output signal at node (3) in MHz to the device bias current in uA . For, this analysis capacitances are fixed at 1pF at $\pm 1V$. The graph appears to be almost linear between 1uA to 2.6uA bias current range. When the bias current is further increased above 2.6uA the frequency increases drastically. The change in the frequency from 2.4uA to 2.8uA is from 58.82 MHz to 100 MHz , which can be a useful in high frequency applications.

Fig 5(b) is the response plotted when device bias current is kept constant at 2uA and the capacitances are changed from 0.5pF to 1.5pF.It has been observed from the graph that the frequency decreases approximately linearly with increase in capacitances.

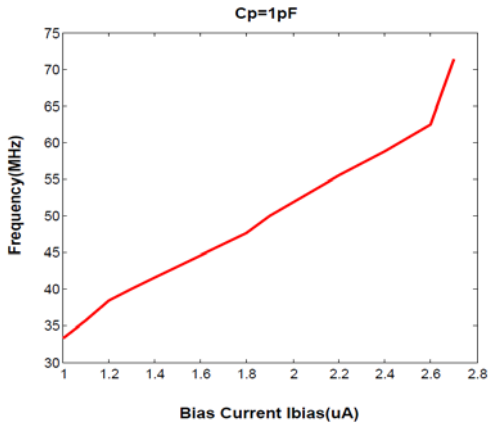

Figure 5: (a) Frequency vs Ibias (Cp=1pF constt.)

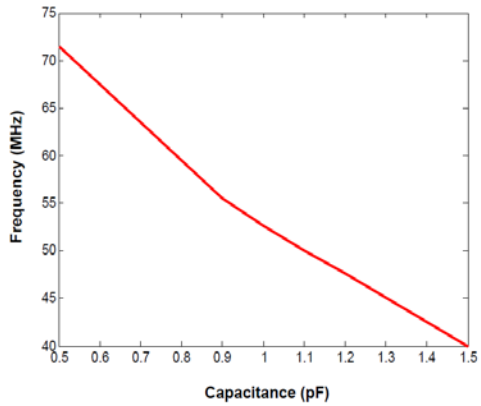

Figure 5: (b) Frequency vs Capacitance (Ibias=2uA constt.)

It is observed from fig.6(a) that the oscillations are started on themselves without applying any trigger signal applied externally. However the oscillation startup time is observed to change with some circuit conditions, like the device bias current,

capacitance. Fig.6(b) below shows this behavior. It has been plotted between oscillator start up time in ns and device bias current in uA between 1uA and 2.2uA. The oscillator starting time is very less from 143ns to approx. 200 ns and after that is increase to 1090 ns which is not feasible for an oscillator to start after such a time delay.In case when the device bias current is kept constant at 2uA then it has been observed that the oscillator startup time increases linearly with the variation of capacitance from 0.5pF to 1.4pF.

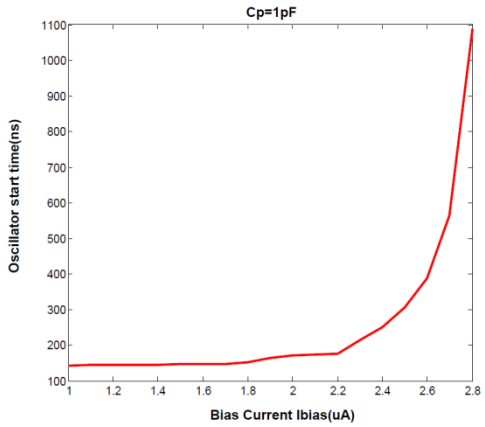

Figure 6(a): Oscillator start time vs Ibias (Cp=1pF constt.).

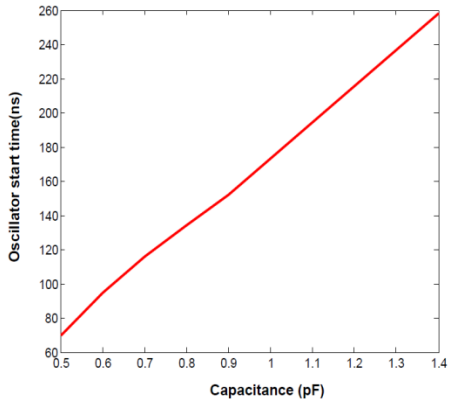

Figure 6(b): Oscillator start time vs Capacitance (Ibias=2uA constt)

The average power of the oscillator is obtained and show in fig 7(a) with variation of bias current keeping capacitance of the device fixed at 1pF and the plot is linearly varied from 1uA to 2.8uA .It has been observed that the average power increases with the increase in the value of device bias current.

When the bias current is kept constant at 2 uA and the average power is obtained with the variation of capacitances it has been observed from the plot of fig.7(b) it has been observed that first the average power decreases with the increase in the

capacitance i.e. for the values from 0.5pF to 1pF after that it has been noticed that the curve start rising at the capacitance value of 1pF and keeps on increasing as the value of the capacitance increases.

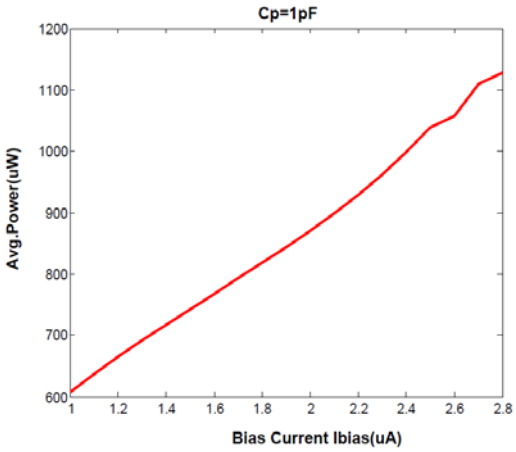

Figure 7(a): Avg Power vs Ibias(Cp=1pF).

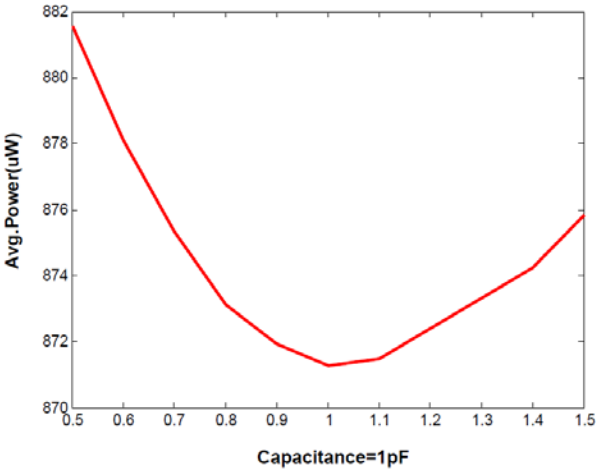

Figure 7(b): Avg.Power vs Capacitance (Ibias=2uA)

Another parameter to study is shown in fig.8(a) that when amplitude is varied in response to device bias current keeping the capacitances constant at 1pF.It has been seen from the plot that the amplitude decreases approx. linearly with the change in bias current from observations been made between the values 1uA to 2.8uA. Now if we vary the capacitance , keeping now the bias current constant at 2uA then it has been seen that a linear decreasing curve is obtained for amplitude as capacitance being varied from 0.5pF to 1.5pF.

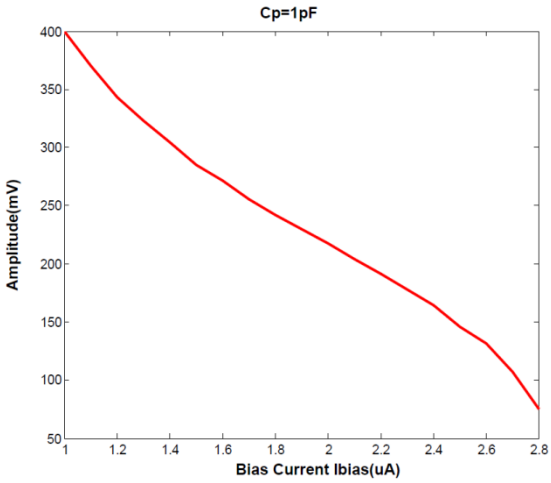

Figure 8(a): Amplitude vs Ibia(Cp=1pF)

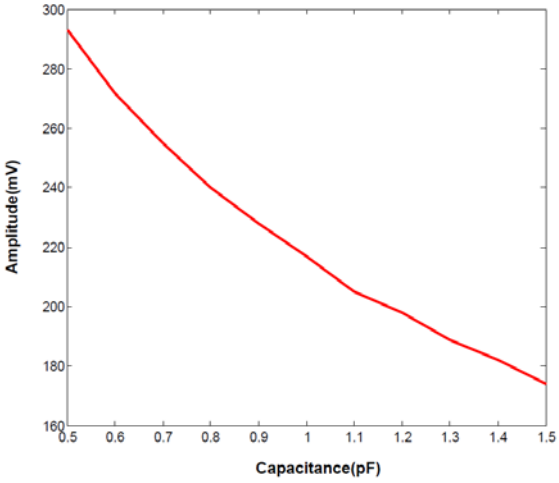

Figure 8(b): Amplitude vs Capacitance(Ibias=2uA)

Figure 9 shows that variation of total harmonic distortion with change of device bias current from 1uA to 2.8uA keeping the capacitance fixed at 1pF.From range between 1uA to 2.7uA the THD remains approx. same but at 2.7uA is increase instantly and the same behavior continues.

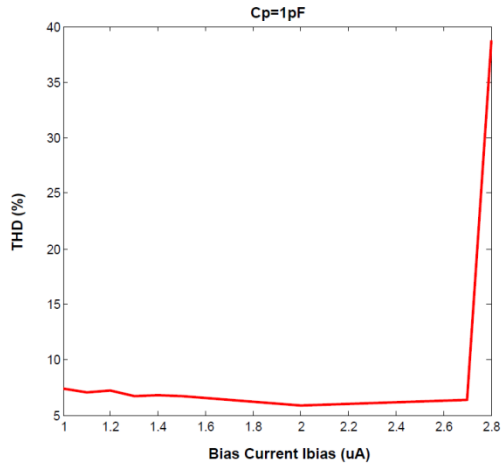

Figure 9: Total Harmonic distortion vs Ibais (Cp=1pF)

Fourier analysis, with respect to the principal frequency (52.6MHz), is performed on the node (3) signal to ascertain the quality of the oscillations. Result of this analysis is presented in figure 10. Peaks in figure 10 correspond to the principal frequency of the oscillator and it's harmonic frequencies. Third harmonic component is significant (-29dB) compared to the second harmonic component (-43dB). Estimates of the total harmonic distortion (THD) and the DC component of the node (3) signal are important quality matrices for the sinusoidal wave shape of the output signal. Both these parameters are found reasonably very low. The simulation results are summarized in Table 1.

It is noteworthy that the sustainable oscillations are established without requiring a trigger signal.

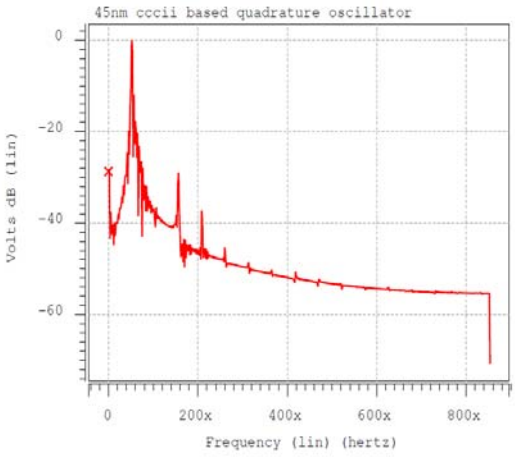

Figure 10: Fourier analysis of the signal at node (3) of fig (3)

Table 1: Performance Results of the Proposed Oscillator

Performance Parameters	Details
Frequency	52.6MHz
Ibias	2uA
Cp	1pF
THD	5.9%
DC Component	-24.2mV
Peak Amplitude	217mV
Avg.Power	871uW
Oscillation startup time	170ns

Conclusion

In this work, a novel oscillator is designed using a single CCCII+, two passive capacitors to control frequency and to sustain the necessary gain. The simulation results of the oscillator verify the circuit capability to generate megahertz oscillations. Quality of oscillations is also reasonable as per the simulation results presented in figures 3 and 10, summarized in Table 1. The DC component of the output is observed about -24.2mV and the total harmonic distortion in the output node (3) signal is about 5.9% at 52.6 MHz frequency (see Table 1). The peak to peak amplitude of the output voltage is 478mV. Also, the simulation shows the average power 871μW when biased through ±1.0V and a 2μA source. The oscillator is also investigated for higher frequencies and found capable of generating 100MHz at I_B=2.8μA, $C_1 = C_2$ = 1pF satisfactorily. It is also supported by the figures 5(a) and 5(b) that smaller capacitance and larger bias current results higher frequency oscillations.

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