Identification of Short Circuit Fault Location in Voltage Source Inverters Based On Rough Set Theory

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Abstract

Fault diagnosis is a complex problem that concerns effective decision-making. However, with the increased complexity of equipments and enrichment in data collection methods, the task of fault diagnosis has become increasingly difficult and its complexity almost unmanageable using traditional techniques. In this paper, a Method of the Rules Extraction for Detection and Identification of Short Circuit Fault Location in Voltage Source Inverters Based on Rough Set Theory is presented. The rough set reduction technique is applied to find all reducts. After that the principles of hypergraph was applied to determine the minimal transversal of reducts. Finally, a set of generalized rules for Short Circuit Fault Location was extracted. The extracted rules are performed with basic logic functions so a digital diagnostic circuit can be obtained. The results show that the presented method can effectively detect and identify the location of faults and do not depend on switch parameters, increase the efficiency and accuracy of diagnosis and can avoid the fault diagnosis dimensional disaster problem.

Keywords: Classification; Rules Extraction ; Fault Diagnosis; Fault Detection; Hypergraph; Rough Set Theory; Feature Selection, Voltage Source Inverter.

I. INTRODUCTION

Fault diagnosis is a complex problem that concerns effective decision-making. Fault diagnosis can be defined as the process of identifying the cause of a malfunction by observing its effects at various monitoring points in a system. Carrying out timely system diagnosis to identify and rectify failure with minimal downtime would help to reduce system maintenance time and improve the overall productivity [1, 2]. With the recent development of the Internet, the Internet of Things, wireless communications, mobile devices, e-commerce, and smart manufacturing, the amount of data collected has grown in an exponential manner. As well as in modern industries, machines have become more automatic, precise and efficient than ever before [3], which makes their health condition monitoring more difficult. To fully inspect the health conditions of the machines, condition monitoring systems are used to collect real-time data from them, and big data are acquired by multiple sensors after the long-time operation. Such explosion of data which generally collected faster than it is analyzed by diagnosticians makes the task of fault diagnosis has become increasingly difficult and its complexity almost unmanageable using traditional techniques. How to effectively extract rules and accurately identify the corresponding health conditions becomes an urgent research subject currently.

The framework of intelligent fault diagnosis includes three main steps: signal acquisition, feature extraction and selection, and fault classification [4]. Feature Extraction aims to extract representative features from the collected signals based on signal processing techniques, like time-domain statistical analysis, Fourier spectral analysis and wavelet transformation [5]. Although these features characterize the health conditions, they may contain useless or insensitive information and affect the diagnosis results as well as computational efficiency. So feature selection is used to select sensitive features through dimension reduction strategies, such as principal component analysis (PCA), distance evaluation technique [6] and feature discriminant analysis [7]. In the fault classification step, the selected features are used to train artificial intelligence techniques like k-nearest neighbor (kNN), artificial neural networks and support vector machine (SVM), fuzzy sets [8-10], rough set theory (RST) [11, 12] which is one of the successful approximation based mathematical model to deal the imprecision and uncertainty present in knowledge. Many heuristic algorithms are proposed based on rough set theory, also numerous approached based on rough set theory and other theories are investigated to extract decision rules and reduce the dimensionality of dataset [13-30].One advantage of the rough set is the creation of readable if-then rules. Such rules have a potential to reveal new patterns in the data material. Thus, the main objective of this work is to present a Method of the Rules Extraction for Detection and Identification of Short Circuit Fault Location in Voltage Source Inverters Based on Rough Set Theory.

II. HYPERGRAPH PRINCIPLE

This section discusses basic definitions of the hypergraph and few exciting properties such as vertex linearity and minimal transversal which can be hybridized with RST to identify the optimal feature subset. According to [31] consider U be a finite set of non-empty elements. If $E = \left((E_i)_{i \in j} \neq \{ \} \right)$ and $\bigcup E_i = V, i \in j$ then $H = (V, E)$ is an hypergraph as shown in fig.

1, where $V = \{v_1, v_2, v_3, \ldots\}$ and $E = \{e_1, e_2, e_3, \ldots\}$ represent the vertices and edges, respectively. Hyperedges of H are represented by $e_i = \{e_{i1}, e_{i2}, e_{i3}, \ldots e_{ij}\}$ $(i \in j; j = 1, 2, 3, \ldots n)$
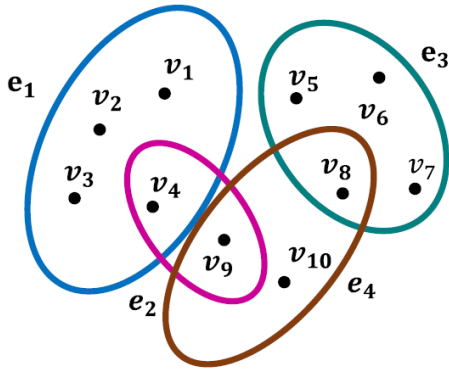

Fig. 1.   Hypergraph structure

According to [32] $H = (V, E)$ for $k \in V$, then set of hyperedges that contain k is known as star of H which is represented as $H(k)$ and degree of k is the cardinality of star $H(k)$ denoted as $k_d = Card(H(k))$. From Fig. 1 $V = \{v_1, v_2, v_3, v_4, v_5, v_6, v_7, v_8, v_9, v_{10}\}$; set of hyperedges $e_1 = \{v_1, v_2, v_3, v_4\}$, $e_2 = \{v_4, v_9\}$, $e_3 = \{v_5, v_6, v_7, v_8\}$, $e_4 = \{v_8, v_9, v_{10}\}$; the star centered on v_8 is $H(k_8) = \{e_3, e_4\}$ and $k_{8d} = 2$; the star centered on v_4 is $H(k_4) = \{e_1, e_2\}$ and $k_{4d} = 2$.

According to [32, 33]:

- $H = (V, E)$ be a simple (Sperner family) only for every $E_a, E_b \in E$; if $E_a \not\subset E_b$, it implies $a \neq b$. The set of $H \subseteq V$ is known as transversal of H only when it intersects every hyperedge of H .

- The transversal hypergraph T_H^r of hypergraph H is a set of all minimal transversals of H .

III. PROBLEM FORMULATION

Single phase inverters are basic inverters which produce a square shape AC output with a DC input. If a DC input is a voltage source, then the inverter is called a Voltage Source Inverter (VSI). These inverters have simple on-off control logic and obviously they operate at much lower frequencies. Voltage source inverters (VSI) are widely used in industrial, aerospace, residential environments, in renewable energy systems, low cost ac motor drives, uninterruptible power supply units(UPS), shunt active power filter, in circuits utilizing electrical resonance between an inductor and a capacitor like induction heating units and electronic ballasts for fluorescent lamps, and in other applications as well. The operation this inverter involves the operating the switches in each leg of the inverter in a complementary manner.

In recent years these inverters have incorporated new technological innovations, nonetheless, they continue to remain susceptible to a variety of failures. Therefore, there is several research studies related to fault-diagnosis methodologies for inverters. Fault diagnosis is divided into two parts: fault detection and fault location. A significant portion of

inverter failure, approximately 31%, occurs in the switches, which are noted among the weak components in power converters [34]. These faults are classified as short-circuit faults, open-circuit faults, and command signal faults. Short-circuit faults in a Voltage source inverters are considered to be serious. There are many methods and techniques used for Short-circuit fault diagnosis , for example, by using neural networks [35] , by using fuzzy logic [36] and methods which based on artificial intelligence, where the input variables are properly conditioned, and from them one can extract the data for constructing the diagnostic rules. The diagnostic accuracy of these methods is dependent upon the knowledge of the system model and its failures in the neural networks methodology. These methods require more time in the detection of the failures due to the signal processing technique used, the complexity of the algorithm, and the computational structure. As well as these methodologies require great computational effort. Other methods for Short-circuit fault diagnosis are embedded in fault-tolerant systems and in this context, the fault diagnosis is followed by reconfiguration of the circuit.

This work presents a Methodology based on rough set theory and hypergraph for generating classification rules to for Detect and Identify of Short Circuit Fault Location in Voltage Source Inverters Based on Rough Set Theory. The proposed method can be used with various types of switches and does not depend on switch parameters. Consider the topology of single phase voltage source Inverter power circuit [37] as shown in Fig. 2. Which represent all the possibilities of measurements of the diverse voltage source inverter quantities related to diagnostic methods, fault detection, or fault location procedures.
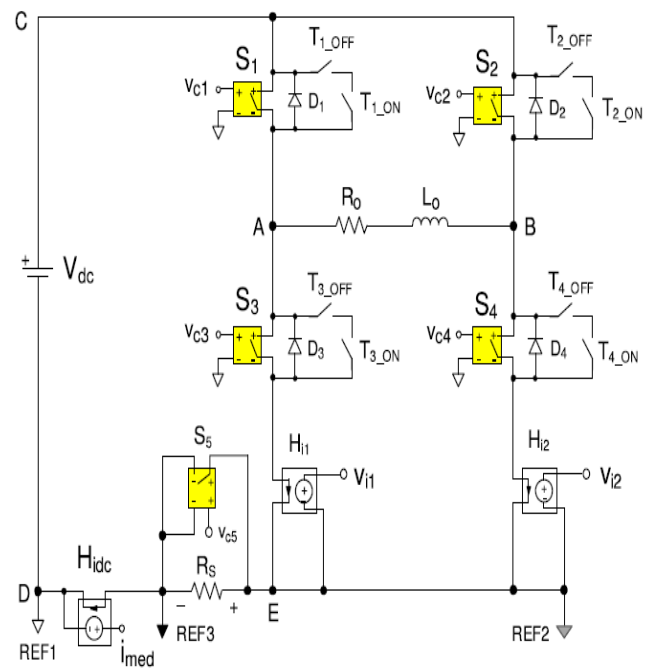

Fig. 2.   Power Circuit Topology of Single Phase Voltage Source Inverte

Here the load current, switches currents, and switches command signals were chosen because these values can be converted to digital logic levels easily and can facilitate the identification of the current circulation path in the voltage source Inverter. The values of currents in the switches and the load are used in defining the operating modes of the inverter. The switches command signals have a pulsed digital signal format and used to determine which switches are enabled for conduction. The waveforms of voltage source inverter operating signals which are chosen to be used as verification signals are shown in Fig.3.
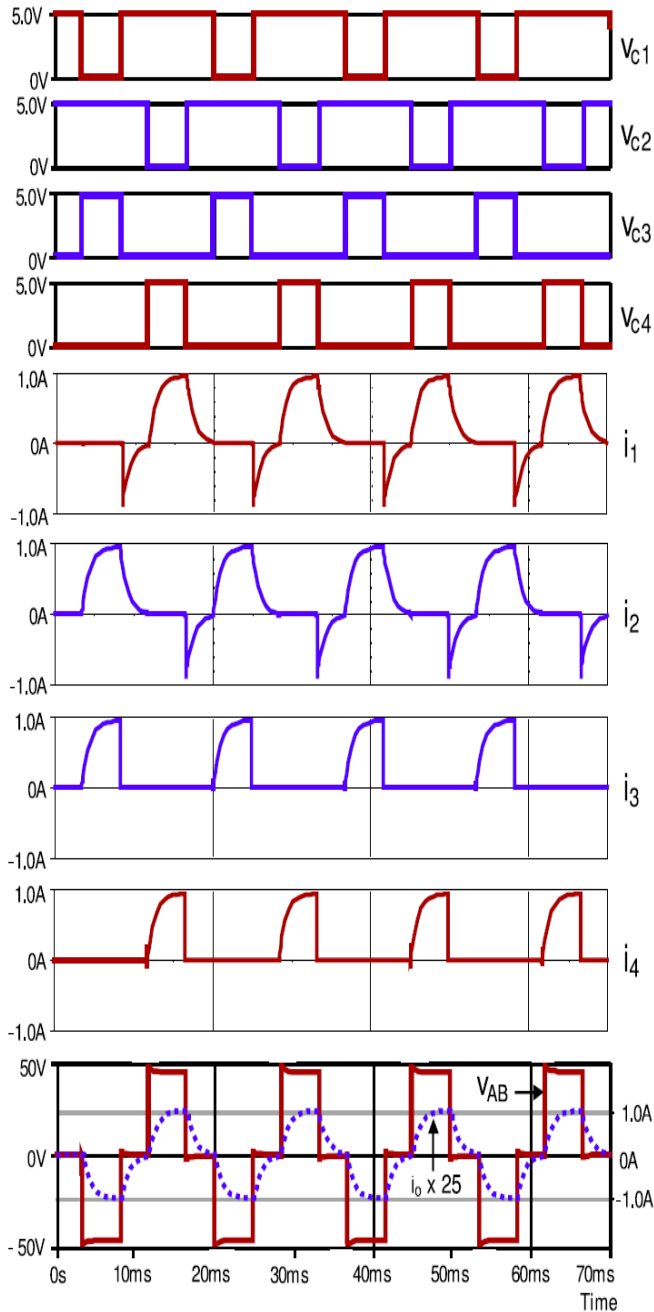

Fig. 3. Waveforms of Voltage Source Inverter Operating Signals

IV. PROPOSED METHODOLOGY

The fault diagnostic variables are: the command voltages of the switches, the currents in the switches and the load current. Table I gives more information about these diagnostic variables (conditional attributes). And the decision table is shown in Table II.

Now, we will discuss the proposed rough sets and hypergraph scheme to analyze, mining and generating diagnostic rules. The main stages will be done with the aid of software called ROSETTA which is an RST analysis toolkit. The rough set reduction technique is applied to find all reducts of the data which contains the minimal subset of attributes that are associated with a class label for classification as shown in Table III.

The next stage is applying the hypergraph principles to determine the minimal transversal of reducts. Consider Fig. 4(a) the hypergraph $H = (V, E)$ where

$V = \{v1,v2,v3,v4,i1,i2,i3,i4,io\}$, $E = \{e_1, e_2, e_3, e_4, e_5\}$; set of hyperedges $e_1 = \{v4, i1, i2\}$, $e_2 = \{v2, i1, i2\}$, $e_3 = \{v1, v2, i2, i3\}$, $e_4 = \{v2, i1, i4, io\}$ $e_3 = \{v1, v2, i2, i3\}$, $e_5 = \{vc2, vc3, i1, i4\}$; the minimal transversal of H hypergraph is $\{\{v2, i1, i2, i4\}, \{v1, v3, v4, i3, io\}\}$. By Considering Fig. 4(b) the hypergraph $H = (V, E)$ where $V = \{v1,v2,v3,v4,i1,i2,i3,i4,io\}$, $E = \{e_6, e_7, e_8, e_9, e_{10}, e_{11}\}$; set of hyperedges $e_6 = \{v2, v3, i2, i3\}$, $e_7 = \{v1, v4, i3, i4\}$, $e_8 = \{v1, v4, i2, i3\}$, $e_9 = \{v3, v4, i2, i3\}$ $e_{10} = \{v4, i1, i4, io\}$, $e_{11} = \{v4, i1, i3, i4\}$; the minimal transversal of H hypergraph is $\{\{v4, i1, i3, i4\}, \{v2, v3, i2\}\}$. By Considering Fig. 4(c) the hypergraph $H = (V, E)$ where $V = \{v1,v2,v3,v4,i1,i2,i3,i4,io\}$, $E = \{e_{12}, e_{13}, e_{14}, e_{15}, e_{16}\}$; set of hyperedges $e_{12} = \{v1, v4, i1, i4\}$, $e_{13} = \{v1, v2, i1, i4\}$, $e_{14} = \{v3, v4, i1, i4\}$, $e_{15} = \{v3, v4, i3, i4\}$ $e_{16} = \{v2, i1, i3, i4\}$; the minimal transversal of H hypergraph is $\{v2, i1, i3, i4\}$.

Finally, the rough sets dependency rules for Detection and Identification of Short Circuit Fault Location in Voltage Source Inverters are generated directly as shown in table IV.

V. DISCUSSION

As shown from the previous sections, the reducts $\{\{v2, i1, i2, i4\}, \{v1, v3, v4, i3, io\}\}$, $\{\{v4, i1, i3, i4\}, \{v2, v3, i2\}\}$, $\{v2, i1, i3, i4\}$ was chosen by the principles of hypergraph. And the decisions rules which extracted using the rough set theory show the isolated Short circuit fault situations in the inverter switches. Table IV contains data that will be used to create the Short circuit fault detection system.

Now we will explain how the proposed method detect the faults, with the voltage source inverter running we collect a set of values from its operation signals to obtain the state of the variable that defines its diagnosis then the diagnosis classification rules shown in table IV will be applied to detect and locate the fault.

In order to evaluate and verify the effectiveness and accuracy of the proposed method, consider the instantaneous values of the operating signals waveforms for the voltage source inverter at the sampling instances shown in Fig.5.
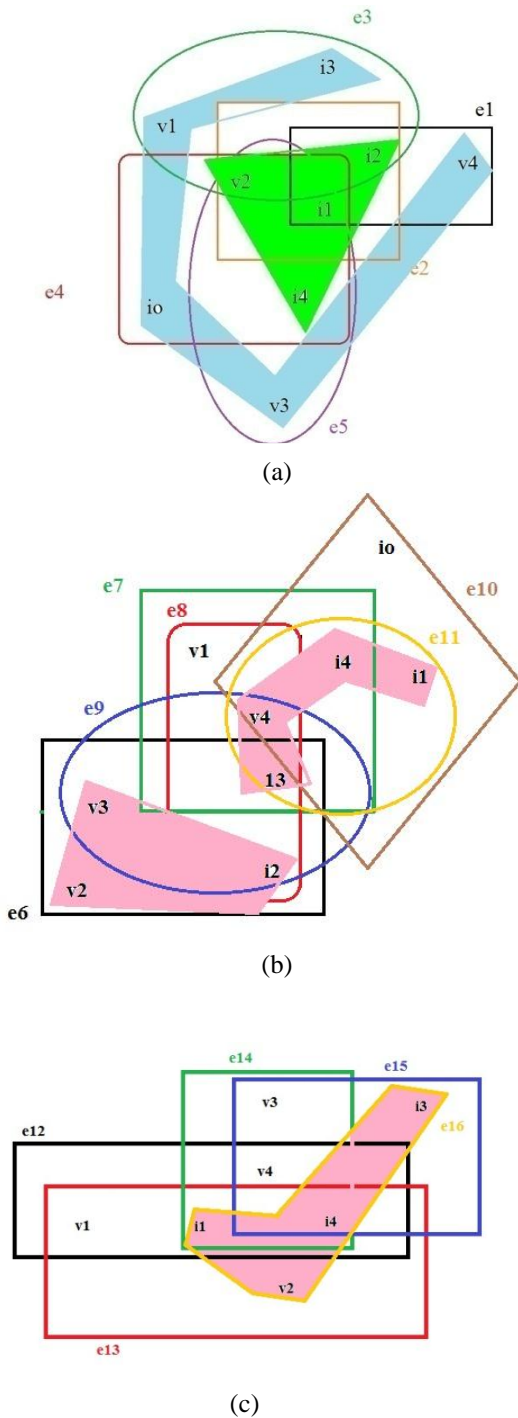
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(a)

(b)

(c)

Fig. 4.: Hypergraphs with minimal transversal property
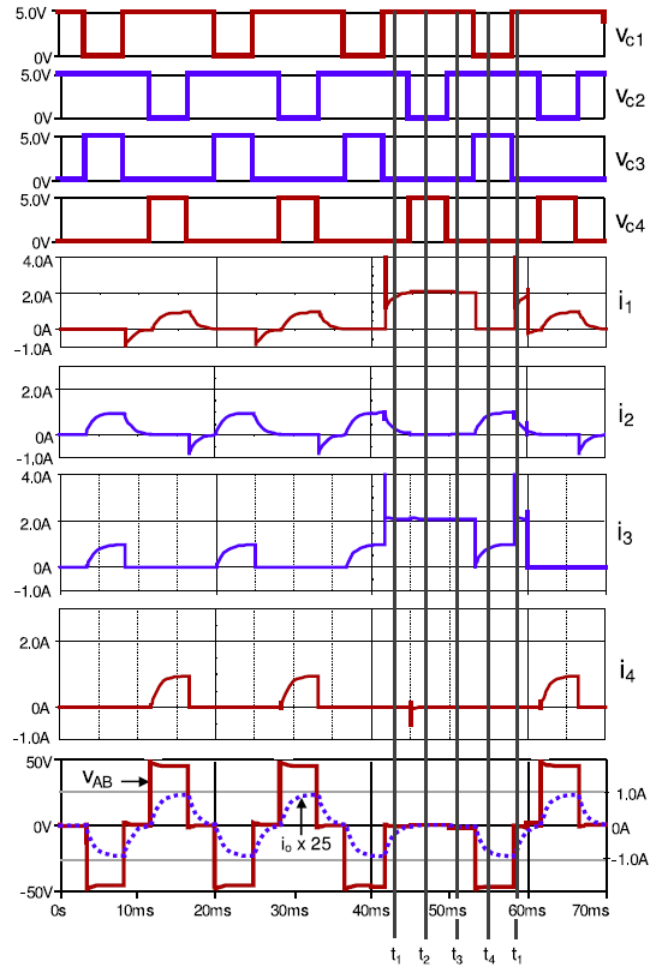

Fig. 5.: the operating signals waveforms for the voltage source inverter at the sampling instances t_1, t_2, t_3, t_4,

In Fig. 6, during the interval from 40 to 60 ms. at the instances (t1, t2, t3, t4, and t1) the instantaneous values of the fault diagnostic variables (the command voltages of the switches, the currents in the switches and the load current) are shown in Table V. The values of the diagnostic variables, referred to Table. IV, indicate that there is a short circuit condition of switch S3. With certainty, we can see that the command voltage vc3 is 0. Then the switch S3 is switched OFF, but its current is ISC.

TABLE V.   INFORMATION FAULT DIAGNOSTIC VARIABLES AT THE INSTANCES (T_1, T_2, T_3, T_4, AND T_1)

U	vc1	vc2	vc3	vc4	i1	i2	i3	i4	io
t1	1	1	0	0	0	0	0	0	0
t2	1	0	0	1	In	0	0	In	In
t3	1	1	0	0	0	0	0	0	0
t4	0	1	1	0	In	0	Isc	0	0
t1	1	1	0	0	0	0	0	0	0

To demonstrate the validity of the proposed method, the results were compared with previously published research [37]. This is done by examining the logic diagnostic circuit proposed by [37] and shown in fig.6, we found great agreement between the results.
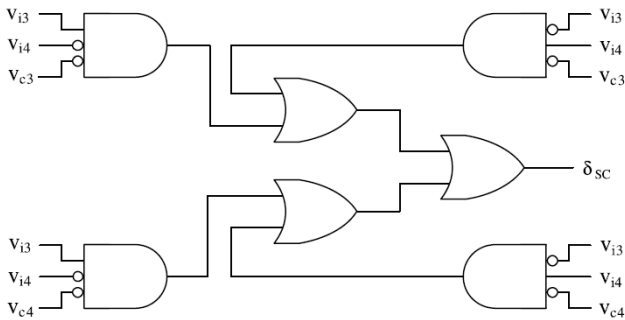

Fig. 6. The logic diagnostic circuit proposed by [35]

VI. CONCLUSION

This paper introduced a methodology for Detect and Identify of Short Circuit Fault Location in Voltage Source Inverters based on rough set theory and hypergraph. The proposed methodology hybridizes the benefits of RST and Sperner hypergraph properties. The minimal transversal properties of hypergraph were exploited on the reducts obtained from RST to identify the informative feature subset of the conditional attributes. The proposed technique has been simplified logic-based rules required to building knowledge. Also it was observed that this system can greatly and effectively reduce both the time and cost. an extension work of using rough sets with other intelligent systems like neural networks, genetic algorithms, fuzzy approaches, and so forth, will be considered in the future work.

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TABLE I.   THE DIAGNOSTIC VARIABLES (CONDITIONAL ATTRIBUTES)

	Attribute	Attribute value
The command voltages of the switches	Vc1	They have two logic levels: 1 (one) : to turn the switch ON 0 (zero) : to turn the switch OFF.
	Vc2	
	Vc3	
	Vc4	
The currents in the switches	i1	They are nonlinear.
	i2	The maximum values are In and ISC.
	i3	In is the nominal current in the N mode.
	i4	ISC is the maximum value of the SC current in the SC mode
The load current	io	Vary from the value 0 to $\pm$In .

TABLE II.   REDUCTS OF TABLE 2.

	Reduct	Support	Length
1	{vc4, i1, i2}	100	3
2	{vc2, i1, i2}	100	3
3	{vc1, vc2, i2, i3}	100	4
4	{vc2, i1, i4, io}	100	4
5	{vc2, vc3, i1, i4}	100	4
6	{vc2, vc3, i2, i3}	100	4
7	{vc1, vc4, i3, i4}	100	4
8	{vc1, vc4, i2, i3}	100	4
9	{vc3, vc4, i2, i3}	100	4
10	{vc4, i1, i4, io}	100	4
11	{vc4, i1, i3, i4}	100	4
12	{vc1, vc4, i1, i4}	100	4
13	{vc1, vc2, i1, i4}	100	4
14	{vc3, vc4, i1, i4}	100	4
15	{vc3, vc4, i3, i4}	100	4
16	{vc2, i1, i3, i4}	100	4

TABLE III.   DECISION TABLE FOR SHORT CIRCUIT FAULT DIAGNOSIS

U	vc1	vc2	vc3	vc4	i1	i2	i3	i4	io	Decision: Short Circuit Failure in Switch
X1	1	1	0	0	0	0	0	0	0	(S1)
X2	1	0	0	1	In	0	0	In	In	(S1)
X3	1	1	0	0	0	0	0	0	0	(S1)
X4	0	1	1	0	In	0	Isc	0	0	(S1)
X5	1	1	0	0	0	0	0	0	0	(S1)
X6	1	1	0	0	0	0	0	0	0	(S2)
X7	0	1	1	0	0	In	In	0	neg In	(S2)
X8	1	1	0	0	0	0	0	0	0	(S2)
X9	1	0	0	1	0	Isc	0	Isc	0	(S2)
X1	1	1	0	0	0	0	0	0	0	(S2)
X1	1	1	0	0	Isc	0	Isc	0	0	(S3)
X1	1	0	0	1	Isc	0	Isc	0	0	(S3)
X1	1	1	0	0	Isc	0	Isc	0	0	(S3)
X1	0	1	1	0	0	In	In	0	neg In	(S3)
X1	1	1	0	0	Isc	0	Isc	0	0	(S3)
X1	1	0	0	1	In	0	0	In	In	(S4)
X1	1	1	0	0	0	Isc	0	Isc	0	(S4)
X1	0	1	1	0	0	Isc	0	Isc	0	(S4)
X1	1	1	0	0	0	Isc	0	Isc	0	(S4)
X2	1	0	0	1	In	0	0	In	In	(S4)

TABLE IV. THE GENERATED RULES TO DETECT AND IDENTIFY OF SHORT CIRCUIT FAULT LOCATION IN VOLTAGE SOURCE INVERTERS

	Rule	LHS SUPPORT	RHS SUPPORT	RHS ACCURACY
1	vc1(1) AND vc2(1) AND i2(0) AND i3(0) => Decision(Short Circuit Failure in Switch (S1)) OR Decision(Short Circuit Failure in Switch (S2))	6	3 ,3	0.5 ,0.5
2	vc1(1) AND vc2(0) AND i2(0) AND i3(0) => Decision(Short Circuit Failure in Switch (S1)) OR Decision(Short Circuit Failure in Switch (S4))	3	2 ,1	,0.333333 0.666667
3	vc1(0) AND vc2(1) AND i2(0) AND i3(Isc) => Decision(Short Circuit Failure in Switch (S1))	1	1	1.0
4	vc1(0) AND vc2(1) AND i2(In) AND i3(In) => Decision(Short Circuit Failure in Switch (S2)) OR Decision(Short Circuit Failure in Switch (S3))	2	1 ,1	0.5 ,0.5
5	vc1(1) AND vc2(0) AND i2(Isc) AND i3(0) => Decision(Short Circuit Failure in Switch (S2))	1	1	1.0
6	vc1(1) AND vc2(1) AND i2(0) AND i3(Isc) => Decision(Short Circuit Failure in Switch (S3))	3	3	1.0
7	vc1(1) AND vc2(0) AND i2(0) AND i3(Isc) => Decision(Short Circuit Failure in Switch (S3))	1	1	1.0
8	vc1(1) AND vc2(1) AND i2(Isc) AND i3(0) => Decision(Short Circuit Failure in Switch (S4))	2	2	1.0
9	vc1(0) AND vc2(1) AND i2(Isc) AND i3(0) => Decision(Short Circuit Failure in Switch (S4))	1	1	1.0
10	vc2(1) AND i1(0) AND i4(0) AND io(0) => Decision(Short Circuit Failure in Switch (S1)) OR Decision(Short Circuit Failure in Switch (S2))	6	3 ,3	0.5 ,0.5
11	vc2(0) AND i1(In) AND i4(In) AND io(In) => Decision(Short Circuit Failure in Switch (S1)) OR Decision(Short Circuit Failure in Switch (S4))	3	2 ,1	,0.333333 0.666667
12	vc2(1) AND i1(In) AND i4(0) AND io(0) => Decision(Short Circuit Failure in Switch (S1))	1	1	1.0
13	vc2(1) AND i1(0) AND i4(0) AND io(neg In) => Decision(Short Circuit Failure in Switch (S2)) OR Decision(Short Circuit Failure in Switch (S3))	2	1 ,1	0.5 ,0.5
14	vc2(0) AND i1(0) AND i4(Isc) AND io(0) => Decision(Short Circuit Failure in Switch (S2))	1	1	1.0
15	vc2(1) AND i1(Isc) AND i4(0) AND io(0) => Decision(Short Circuit Failure in Switch (S3))	3	3	1.0
16	vc2(0) AND i1(Isc) AND i4(0) AND io(0) => Decision(Short Circuit Failure in Switch (S3))	1	1	1.0
17	vc2(1) AND i1(0) AND i4(Isc) AND io(0) => Decision(Short Circuit Failure in Switch (S4))	3	3	1.0
18	vc2(1) AND vc3(0) AND i2(0) AND i3(0) => Decision(Short Circuit Failure in Switch (S1)) OR Decision(Short Circuit Failure in Switch (S2))	6	3 ,3	0.5 ,0.5
19	vc2(0) AND vc3(0) AND i2(0) AND i3(0) => Decision(Short Circuit Failure in Switch (S1)) OR Decision(Short Circuit Failure in Switch (S4))	3	2 ,1	,0.333333 0.666667
20	vc2(1) AND vc3(1) AND i2(0) AND i3(Isc) => Decision(Short Circuit Failure in Switch (S1))	1	1	1.0
21	vc2(1) AND vc3(1) AND i2(In) AND i3(In) => Decision(Short Circuit Failure in Switch (S2)) OR Decision(Short Circuit Failure in Switch (S3))	2	1 ,1	0.5 ,0.5

	Rule	LHS SUPPORT	RHS SUPPORT	RHS ACCURACY
22	vc2(0) AND vc3(0) AND i2(Isc) AND i3(0) => Decision(Short Circuit Failure in Switch (S2))	1	1	1.0
23	vc2(1) AND vc3(0) AND i2(0) AND i3(Isc) => Decision(Short Circuit Failure in Switch (S3))	3	3	1.0
24	vc2(0) AND vc3(0) AND i2(0) AND i3(Isc) => Decision(Short Circuit Failure in Switch (S3))	1	1	1.0
25	vc2(1) AND vc3(0) AND i2(Isc) AND i3(0) => Decision(Short Circuit Failure in Switch (S4))	2	2	1.0
26	vc2(1) AND vc3(1) AND i2(Isc) AND i3(0) => Decision(Short Circuit Failure in Switch (S4))	1	1	1.0
27	vc4(0) AND i1(0) AND i3(0) AND i4(0) => Decision(Short Circuit Failure in Switch (S1)) OR Decision(Short Circuit Failure in Switch (S2))	6	3 ,3	0.5 ,0.5
28	vc4(1) AND i1(In) AND i3(0) AND i4(In) => Decision(Short Circuit Failure in Switch (S1)) OR Decision(Short Circuit Failure in Switch (S4))	3	2 ,1	,0.333333 0.666667
29	vc4(0) AND i1(In) AND i3(Isc) AND i4(0) => Decision(Short Circuit Failure in Switch (S1))	1	1	1.0
30	vc4(0) AND i1(0) AND i3(In) AND i4(0) => Decision(Short Circuit Failure in Switch (S2)) OR Decision(Short Circuit Failure in Switch (S3))	2	1 ,1	0.5 ,0.5
31	vc4(1) AND i1(0) AND i3(0) AND i4(Isc) => Decision(Short Circuit Failure in Switch (S2))	1	1	1.0
32	vc4(0) AND i1(Isc) AND i3(Isc) AND i4(0) => Decision(Short Circuit Failure in Switch (S3))	3	3	1.0
33	vc4(1) AND i1(Isc) AND i3(Isc) AND i4(0) => Decision(Short Circuit Failure in Switch (S3))	1	1	1.0
34	vc4(0) AND i1(0) AND i3(0) AND i4(Isc) => Decision(Short Circuit Failure in Switch (S4))	3	3	1.0
35	vc2(1) AND i1(0) AND i3(0) AND i4(0) => Decision(Short Circuit Failure in Switch (S1)) OR Decision(Short Circuit Failure in Switch (S2))	6	3 ,3	0.5 ,0.5
36	vc2(0) AND i1(In) AND i3(0) AND i4(In) => Decision(Short Circuit Failure in Switch (S1)) OR Decision(Short Circuit Failure in Switch (S4))	3	2 ,1	,0.333333 0.666667
37	vc2(1) AND i1(In) AND i3(Isc) AND i4(0) => Decision(Short Circuit Failure in Switch (S1))	1	1	1.0
38	vc2(1) AND i1(0) AND i3(In) AND i4(0) => Decision(Short Circuit Failure in Switch (S2)) OR Decision(Short Circuit Failure in Switch (S3))	2	1 ,1	0.5 ,0.5
39	vc2(0) AND i1(0) AND i3(0) AND i4(Isc) => Decision(Short Circuit Failure in Switch (S2))	1	1	1.0
40	vc2(1) AND i1(Isc) AND i3(Isc) AND i4(0) => Decision(Short Circuit Failure in Switch (S3))	3	3	1.0