Design and Performance Optimization of a Wide Band Millimeter-wave Power Amplifier in 130 nm SiGe BiCMOS Technology

First Siddig Gomha[1,2],   Kibet Langat[1,3]

[1]*Department of Electrical Engineering, Pan African University,
Institute for Basic Sciences Technology and Innovation PAUSTI, Nairobi, Kenya.*

[2]*Faculty of Engineering, University of Medical Sciences and Technology,
P.O. Box 12810, Khartoum, Sudan.*

[3]*Department of Telecommunication and Information Engineering,
Jomo Kenyatta University of Agriculture and Technology, Nairobi, Kenya.*

Abstract

This paper presents simple systematic way of designing and optimizing of a wide band millimeter-wave power amplifier using IHP 130 nm SiGe BiCMOS Technology, for applications that operate between 50 – 65 GHz and requires a high data rate. Single stage common emitter configuration with multiple emitter fingers are investigated, five configurations with variable number of emitter fingers are studied separately. A load-pull technique is used for determining the optimal input, output impedance at maximum output power as well as maximum power added efficiency (PAE). Based on the load-pull analysis, an input, output impedance matching network is designed for each configuration. Thereafter, the performance of single stage PA like gain, efficiency, PAE, and 1-dB compression are compared. Based on this comparison, a configuration of six emitter fingers is selected for designing three stages power amplifier, The three stages PA has a gain of 21 dB, PAE of 20.5%, saturation output power of 6.7 dBm, and reflections S_{11}, S_{22} >-10 dB for the band width of (50 – 65 GHz) with unconditionally stability.

Keywords: Optimizing impedance matching network; Power Amplifier; Wide Band Millimeter-wave Power Amplifier.

I. INTRODUCTION

The unlicensed frequency band around 60 GHz attracts many applications in Industrial, Scientific and Medical ISM [1], such as Automotive Radar [2], [3], HD wireless [4], and point to point Gb/s communication [5]. Due to the high attenuation of signal in the band of (56 – 64 GHz), this frequency band is only suitable for short range wireless communication as indoor applications. A power amplifier (PA) plays an essential role in the above mentioned applications for boosting the power of transmitted signal and satisfying the link budget in a communication link. Because of the shrinking transistor size, the break down voltage of transistor will decrease at high frequency and voltage supply (Vcc) will be very limited, therefore, enhancing the power of transmitted signal is

become more challenged [6]. SiGe BiCMOS technology provides many advantages for millimeter-wave applications when compared by a CMOS technology in term of cost, operating voltage, power handling capability, linearity and impedance matching [7]. Many researches have been carried out to enhance the performance of power amplifier like linearity [8]–[11], gain, output power, and efficiency [12]–[15] using different process technologies and circuit topologies. In this paper, a very simple systematic way for designing a multi-stage power amplifier based on optimizing the accurate values of components for the input, output impedances matching as well as inter-stage matching is presented. First of all, ideal components are used for design and optimize the accurate values of lumped components, the performance shows a good progress after optimizing the input, output and inter-stage matching circuits. Thereafter, the ideal lumped components are replaced by the IHP modeled components, ideal capacitor replaced by Metal-Insulator-Metal MIM capacitor as well as inductors replaced by microstrip transmission lines, the ADS is used for design and simulation the PA, it use 1.2 V DC supply and 0.85 V biasing voltage. The paper is organized as follows: section II presents design of a single stage PA by investigating the performance of PA with varying the number of emitter fingers while section III presents an optimizing the performance of multi-stage PA for six emitter fingers. In section IV, the ideal components of the modelled multi-stage PA are replaced by components provided by the foundry. Section V gives conclusion and future work.

II. DESIGN OF SINGLE STAGE PA WITH VARIABLE NUMBER OF EMITTER FINGERS

IHP foundry provides features such as variable number of emitter fingers for the 130nm BiCMOS transistor. There are two options for transistor length: 0.48 and 0.84 μm with multiple emitter fingers. This configuration has up to eight fingers. Despite the highlighted advantage, the transistor with 0.48 μm length of emitter is the best option because it has lowest base resistance. The maximum number of emitter

fingers is eight. However, two or more transistors can be connected in a parallel manner to increase the number of fingers, therefore increasing the overall transistor current. According to [16], a collector current of 1.2 mA can be obtained from a transistor with one emitter finger in order to obtain a maximum transition frequency f_{max} of (340 GHz) with a supply voltage of (V_{CC} =1.2 V) and (V_{BB} = 0.85 V) bias voltage.

1.1 IMPEDANCE MATCHING USING LUMPED COMPONENTS

To ensure the delivery of maximum power from source to load of a power amplifier, the real parts of the source and load impedance should be equal. The source and load impedances should also be conjugate matched, i.e. the imaginary parts must be equal with opposite polarity [17]. There are many techniques for impedance matching such as transmission line matching, transformer matching, and lumped components matching. The later is used in this work to match the impedance of the input and output of the single PA and it is also useful for the inter-stage matching of the multi-stage PA. Figure 1 shows how to use lumped components in Smith chart to implement matching network. Impedance transformation from any point in the Smith chart to 50Ω requires at least two components.
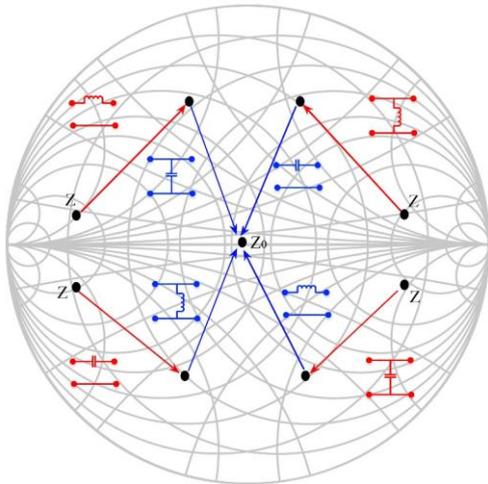
Figure 1: Impedance matching transformation using capacitors and inductors.

1.2 LOAD PULL UTILITY IN ADS

Load pull is a technique for determining the optimum load impedance corresponding a particular output power and PAE for a power amplifier device. Load pull simulation tool in ADS is a very powerful tool for visualizing tradeoff between PAE and delivered power [18]. Furthermore, it is an analysis tool used to drawing a set of contour circles on the Smith chart for the maximum delivered power and PAE achievable for specific load impedance, as shown in Figure 2. The red and blue contour circles on the Smith chart represent the delivered power and the percentage of PAE% respectively. The left side plot shows the relation between PAE and

delivered power. The rectangle with a red border shows the correspondence values of Z_{load} and Z_{in} impedance for the tested transistor which is equal to (100-j9) for Z_{load} and (38.37-j4.23) for Z_{in}. These impedance values have been used for designing input and output matching networks as shown in Figure 3.
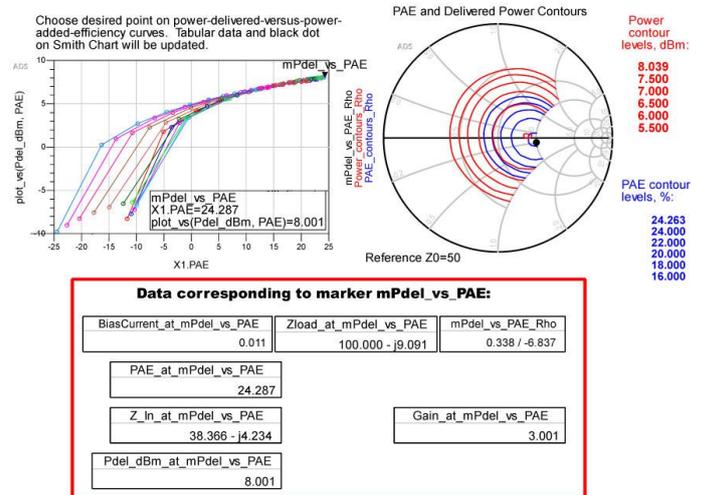
Figure 2: Transistor input impedance and load impedance corresponding the maximum power delivered and PAE%.

Five different configurations with variable numbers of emitter fingers have been considered in this study. One transistor can support up to eight fingers, therefore, one transistor with 3, 6, 8 fingers and two transistors connected in parallel with 12, and 16 fingers are investigated. All transistors have a 0.48 μm emitter length. The common emitter (CE) topology was used for designing the PA with 1.2 V voltage supply and 0.85 V bias voltage. By using Smith chart utility in ADS simulator, the input and output impedance match circuits have been accomplished and inserted into the schematic circuit as shown in Figure 3.
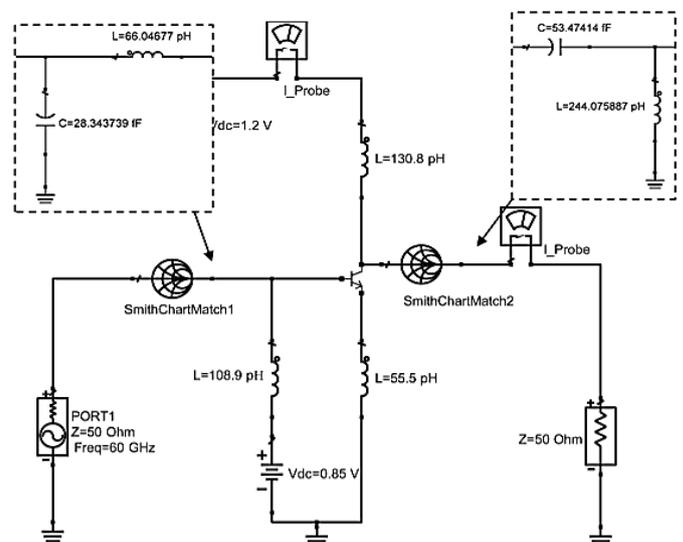
Figure 3: Input and output impedance matching test bench.

The schematic circuit shown in Figure 3 was used as a test bench for the simulation of all proposed PA with a varying number of emitter fingers. The Smith chart symbol in the input and output of the circuit are used for designing and testing impedance matching network for each PA. The large-signal behaviour of a power amplifier such as Gain (G), Effeciency (η), and PAE can be calculated as:

$$Power\ Gain = \frac{P_L}{P_{in}} \qquad (1)$$

$$\eta = \frac{P_{out}}{P_{DC}} \qquad (2)$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \left(1 - \frac{1}{G}\right)\eta \qquad (3)$$

Where, P_L, P_{in}, P_{out}, P_{DC}, and η are power dissipated in the load, power deliverd to the input, output power, DC input power, and effeciency respectively.

1.3 PERFORMANCE COMPARISON OF A SINGLE STAGE PA WITH VARIABLE NUMBER OF EMITTER FINGERS

A comparison of large-signal behavior for all PA design configurations are studied. Figure 4 depicts a comparison of gain when using varying number of emitter fingers. It has been observed that a PA with a small number of emitter fingers (less than 3) produces a lower gain, while a PA with large number of fingers produces a high gain, this is because the collector current and the output power decrease with few emitter fingers, therefore decreasing the transistor gain.
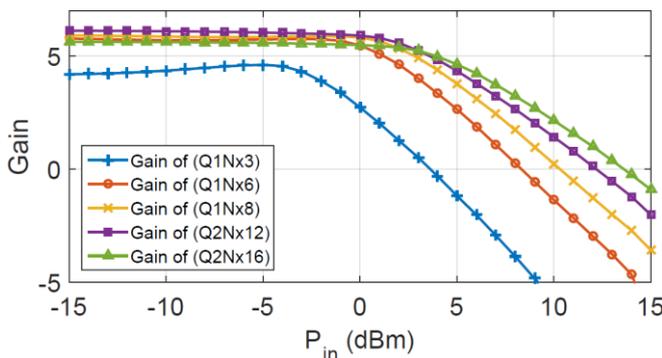
Figure 4: Gain comparison for the PA with a varying number of emitter fingers.

Figure 5. Shows the relationship between input power P_{in} (dBm) and PAE (%) with varying number of emitter fingers. From the plot, a smaller number of emitter fingers results in a lower PAE (%) and vice versa, because efficiency is directly proportional with output power as well as PAE as mentioned in equations (2), and (3) above.
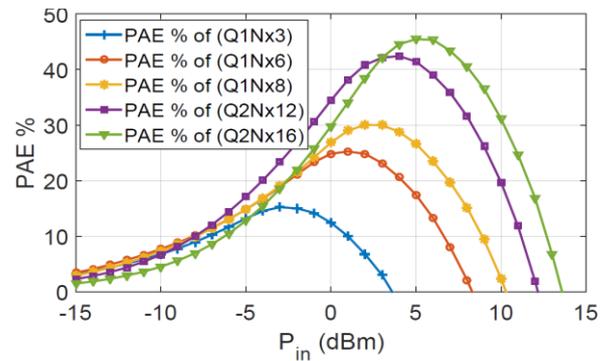
Figure 5: PAE (%) comparison for the PA with a varying number of emitter fingers.

Figure 6. depicts the saturated output power coupled with 1 dB compression for the PA with varying number of emitter fingers. An increse in emitter fingers provide more output power, therefore enhancing the 1 dB compression, consequently enhancing the linearity of PA.
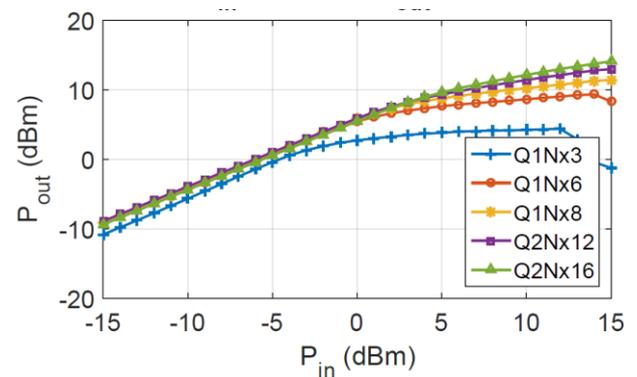
Figure 6: A plot of P_{out} vs. Pin with a varying number of emitter fingers.

In Table 1, performance comparison for the single stage PA with varying number of emitter fingers is tabulated.

Table 1: Summarizing performance comparison of single stage PA with varying number of emitter fingers.

Number of Transistor Q	Number of emitter fingers (N)	Gain	PAE%	P_{sat}	1dB compression
1	3 (Q1_Nx3)	4	20	4.1	2.38
1	6 (Q1_Nx6)	5.8	28	9	6.62
2	8 (Q1_Nx8)	5.9	31	11.5	7.9
2	12 (Q2_Nx12)	6	42	13	8.1
2	16 (Q2_Nx16)	5.6	45	15	9.6

Based on the varying number of emitter fingers explored above, a six emitter fingers was selected for designing and optimizing a single stage PA. Increasing number of emitter

fingers will increase the current densities that will tend to decrease reliable operation, consequently decreasing device performance [7]. Figure 7, shows the schematic circuit of the PA with input and output impedance matching circuits after optimizing the values of inductors and capacitors. The PA was biased at 0.85 V with DC supply equal to 1.2 V, and at 60GHz frequency. The optimization procedure was conducted on ADS simulator using Quasi-Newton method, which is a very fast optimization technique. Figure 8 shows the simulating results of the small-signal S-parameters (left), as well as large-signal behavior (right) for gain, PAE, and efficiency. The PA achieves a gain (S_{21}) of 7.8 dB, and reflections S_{11}, S_{22} are $> $-10dB between a bandwidth of $55 - 65$ GHz, the PAE along with collector efficiency are 40%, and 57% respectively.
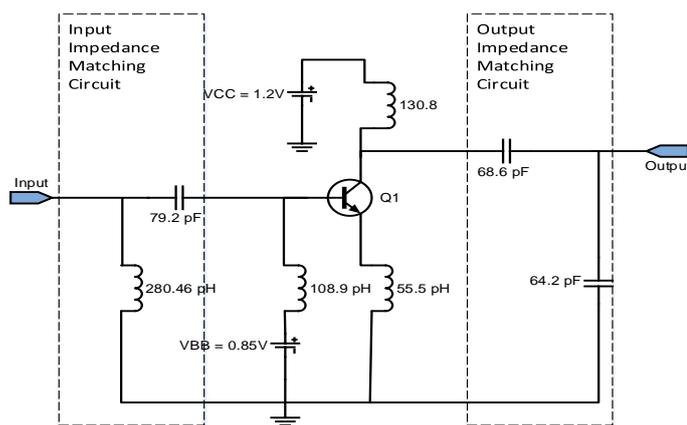
Figure 7: Single stage PA schematic circuits with optimized values of components for input and output impedance matching.
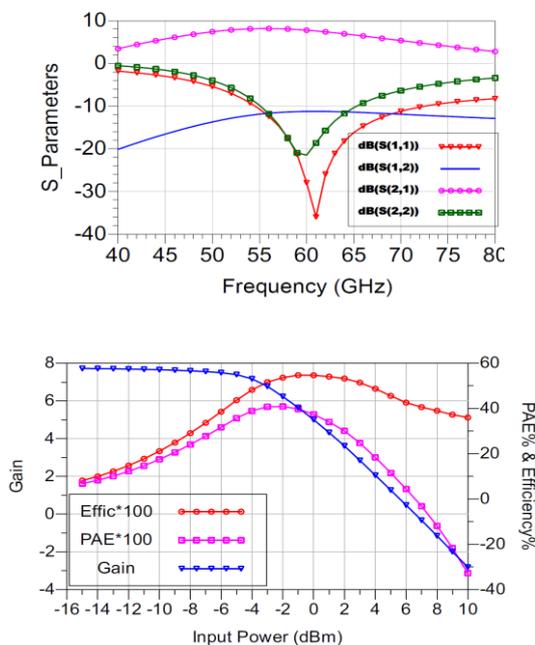
Figure 8. Simulated result of small-signal S-parameters (left), and large-signal behavior (right) for the optimized single stage PA.

OPTIMIZING THE PERFORMANCE OF MULTI-STAGE PA FOR SIX EMITTER FINGERS

Single stage PA has a very limited performance, particularly in high frequency bands. Therefore, employing two or more stages is required for enhancing gain, linearity, and efficiency. However, such parameters should be considered when designing multistage PA for millimeter wave applications, because tight trade-off exists between gain, linearity, and efficiency, at a higher carrier frequency. Maximum output power probably will make the trade-off between efficiency and linearity very tight. High linearity design will tend to lower gains. Furthermore, providing thick metal layers from the foundry will reduce the loss of on-chip components like inductors and transmission line, and also at high frequencies, skin effect will be dominant and availability of thick metal layers become less important. In addition, there is a trade-off between using of-chip matching impedance circuits and chip area in PA designs [19]. All the above mentioned factors will directly affect the overall performance of PA.

Moreover, transistor size for each PA stage has significant effects on the performance of a multi-stage PA. It is a common trend to use smaller transistor size for driver and pre-driver stage, while using bigger transistor size for the output stage to maximum output power, as discovered in [6], [20], [21]. As long as a driver stage is bigger than required size, it will adversely affect the PAE, and if it is lower than required size, it will never provide sufficient power for the last stage to achieve the maximum delivered power. On the other hand, using smaller transistor in the driver stage will tend to compress the signal before the second stage, because the second stage has low input impedance and small transistor needs a larger load resistance. Consequently, impedance transformation will be very high which will tend to high signal losses. Therefore in this paper, equal size transistors have been considered for all stages of the PA. In a multi-stages PA, performance of unit cell single stage PA will directly affect on the overall performance of gain, PAE, and output power. Therefore, the overall performance has been enhanced by optimizing input and output impedance as well as inter-stage impedance.

Efficiency of PA measures the ability of device in converting DC power to RF power. When the efficiency is high, the device consume less power for converting DC power to RF power while at low efficiency, device consume more power and drain storage battery very fast, as well as generating heat. In multi-stages PA, the output stage contribute the highest efficiency, because it has higher output power. Despite this advantage, it results in poor linearity. Therefore, it will be better to work close to a compression as much as possible to obtain the required efficiency. In addition, driver stage generate lower output power, hence their contribution in overall efficiency is smaller. For multi-stages PA, the overall PAE (PAE_{total}) can be calculated as [22]:

$$PAE_{total} = \frac{P_o}{V.(\sum_{i=1}^{N} I_i)}.\left[1 - \frac{1}{\prod_{n=1}^{N} G_n}\right].100 \qquad (4)$$

The total PAE for two stages can be calculated as:

$$PAE_{total} = \frac{P_{o2}}{V.(I_1+I_2)}.\left[1-\frac{1}{G_1 G_2}\right].100 \qquad (5)$$

Where, G_1, and G_2 are the gain of first and second stage; V is the DC supply, I_1, and I_2 are the current as shown in Figure 9. I_1 and I_2 can be calculated as:

$$I_1 = 100.P_{o1}.\left[\frac{(G_1-1)}{PAE_1.V.G_1}\right], \quad I_2 = 100.P_{o2}.\left[\frac{(G_2-1)}{PAE_2.V.G_2}\right] \qquad (6)$$
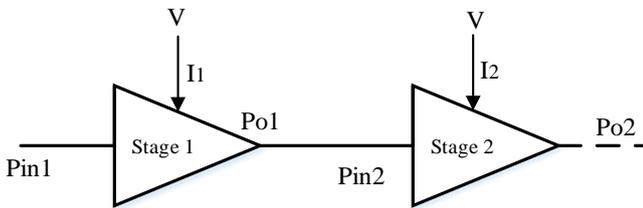
Figure 9: Cascaded multi-stage PA.

The Power Added Efficiency of driver (PAE_1), and output (PAE_2) stages can be calculated as:

$$PAE_1 = \frac{P_{o1}}{V.(I_1)}.\left[1-\frac{1}{G_1}\right].100 \ ,$$

$$PAE_2 = \frac{P_{o2}}{V.(I_2)}.\left[1-\frac{1}{G_2}\right].100 \qquad (7)$$

Figure 10 shows the block diagram of three stages PA with schematic circuits of each block. The PA consist of CE transistor with six fingers for each stage, as well as input, output and inter-stage matching circuits using lumped components. The circuit supplied by 1.2 V, biased at 0.85 V, and working around 60 GHz. The components of impedance matching networks have been optimized in two steps to enhance the overall performance of PA. In the first step, the components of the inter-stage were optimized. Thereafter, the components of input and output matching circuits are optimized.
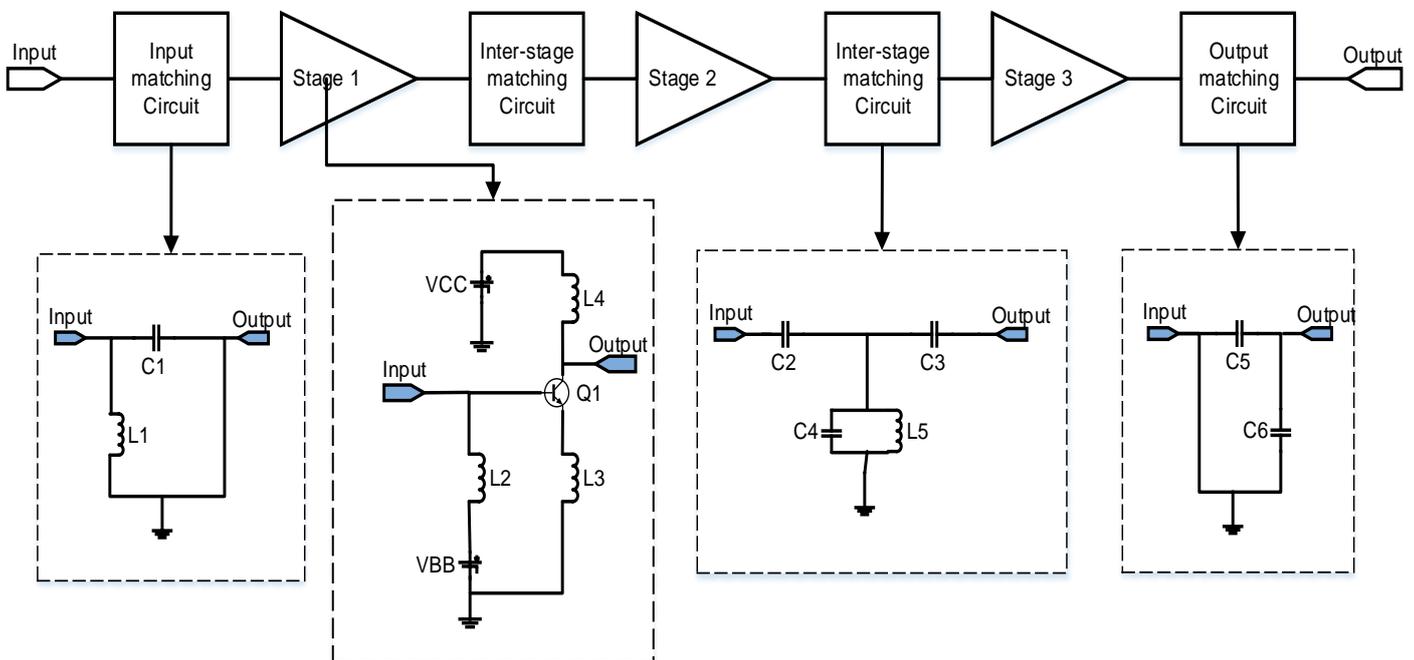
Figure 10: Block diagram with schematic circuits for the cascaded three-stage PA.

The optimized single stage PA shown in Figure 7 has been considered as a unit cell for designing the three stages PA without any optimization for the components of impedance matching networks. Figure 11 shows the *S*-parameters (left), and large-signal behavior (right) before optimization. At frequency band (45 - 60) GHz, the reflections S_{11}, and S_{22} are less than -8.6 dB, while gain, PAE, efficiency, P_{sat}, and 1_{dB} compression are 21, 28.7%, 28.7%, 6, and 3.9dBm respectively.
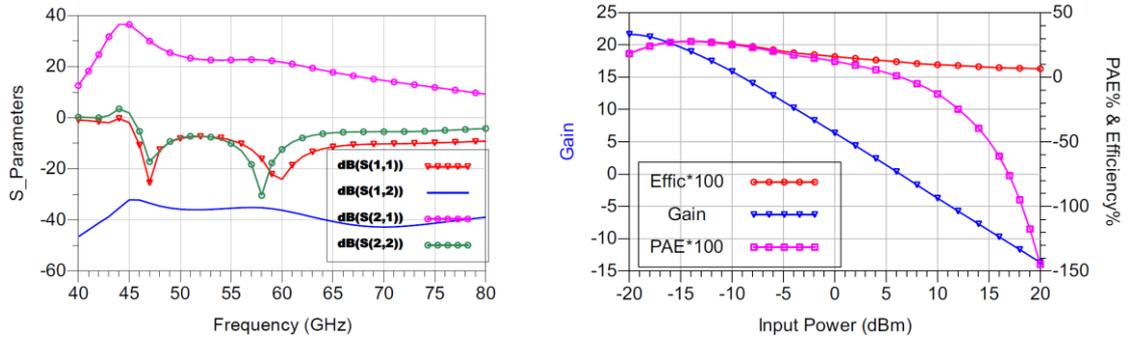
Figure 11: Simulated result of small-signal S-parameters (left), and large-signal behavior (right) for the three stages PA without optimization of impedance matching networks.

After inter-stage optimization, the frequency band has been shifted to 50 GHz – 65 GHz. In Figure 12, the *S*-parameters (left), and large-signal behavior (right), the reflections S_{11}, and S_{22} are less than -9 dB, while gain, PAE, efficiency, P_{sat}, and 1_{dB} compression are 21, 30%, 30%, 6.7, and 4.2 dBm respectively. From these results, it can be observed that all parameters have been improved at frequency band around 60 GHz.
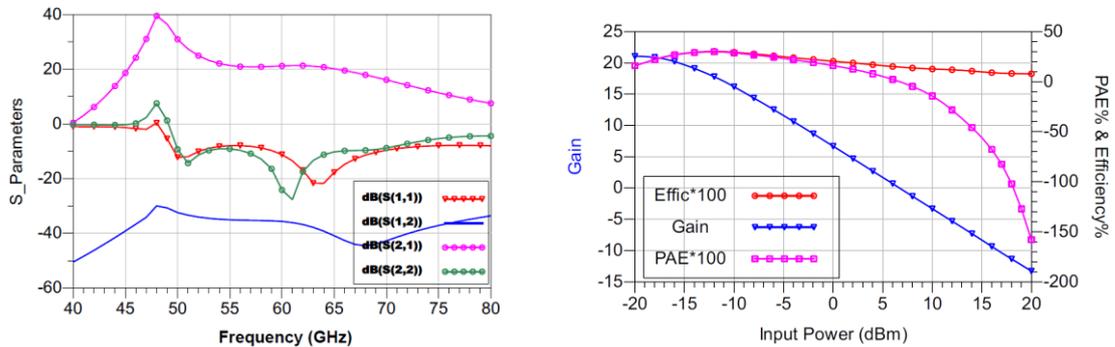
Figure 12: Simulated result of small-signal S-parameters (left), and large-signal behavior (right) for the three stages PA after optimizing inter-stage matching components.

In addition, the input and output matching components have been optimized. After this optimization step, the PA fulfill the best performance, as shown in Figure 13. The reflections S_{11}, and S_{22} are about -12.5 dB, while gain, PAE, efficiency, P_{sat}, and 1_{dB} compression are 21, 32%, 32%, 7.7, and 5.2 dBm respectively.
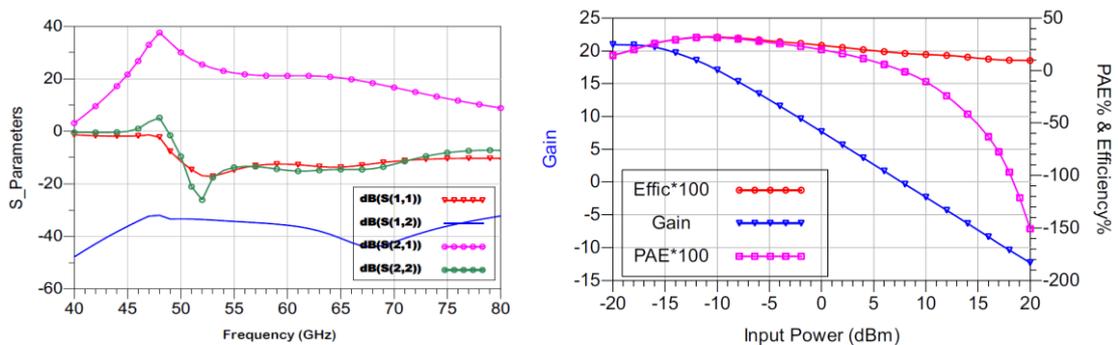
Figure 13: Simulated result of small-signal S-parameters (left), and large-signal behavior (right) for the three stages PA after optimizing inter-stage, input, and output matching components.

Table 2 shows the value of lumped components used for designing the three stages PA. Three cases were considered: before optimization, after inter-stage optimization, and after input and output optimization. In addition, the performance comparison for the three cases shown in Table 3, and Figure 14 shows the progress of P_{sat} for the three causes.

Table 2: The value of components for the three cases, before optimization, after inter-stage optimization, and after input and output optimization.

	Circuit components	Before optimization (case 1)	After inter-stage matching optimization (case 2)	After input, output matching optimization (case 3)
Inter-stage matching components	C2 fF	68.6	128.57	No change
	C3 fF	64.2	45.47	No change
	C4 fF	79.2	195.44	No change
	L5 pH	280.46	40.28	No change
Input matching components	C1 fF	79.2	No change	55.41
	L1 pH	280.46	No change	212.44
Output matching components	C5 fF	68.6	No change	80.18
	C6 fF	64.2	No change	43.81
Main circuit components	L2 pH	108.9	No change	No change
	L3 pH	55.5	No change	No change
	L4 pH	130.8	No change	No change
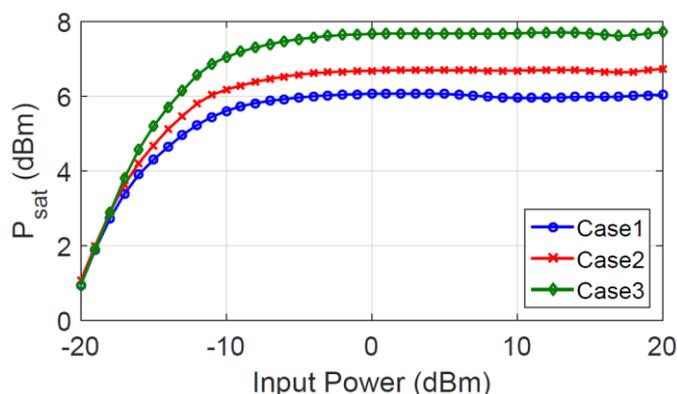
Figure 14: Progress in output power saturation (P_{sat}) for the three cases, before optimization (case 1), after inter-stage optimization (case 2), and after input and output optimization (case 3).

Table 3: Performance comparison for the three cases, before optimization, after inter-stage optimization, and after input and output optimization.

	Before optimization (case 1)	After inter-stage matching optimization (case 2)	After input, output matching optimization (case 3)
Bandwidth GHz	45 – 60	50 - 65	50 – 65
S_{11} dB	-8.6 @ (45 – 60) GHz	-9 @ (50 – 65) GHz	-12.5 @ (50 – 65) GHz
S_{22} dB	-8.6 @ (45 – 60) GHz	-9 @ (50 – 65) GHz	-12.5 @ (50 – 65) GHz
S_{21} dB	21 @ (45 – 60) GHz	20 @ (50 – 65) GHz	20 @ (50 – 65) GHz
Gain	21	21	21
PAE %	28.7	30	32
Efficiency %	28.7	30	32
P_{sat} dBm	6	6.7	7.7
1_{dB} compression dBm	3.9	4.2	5.2
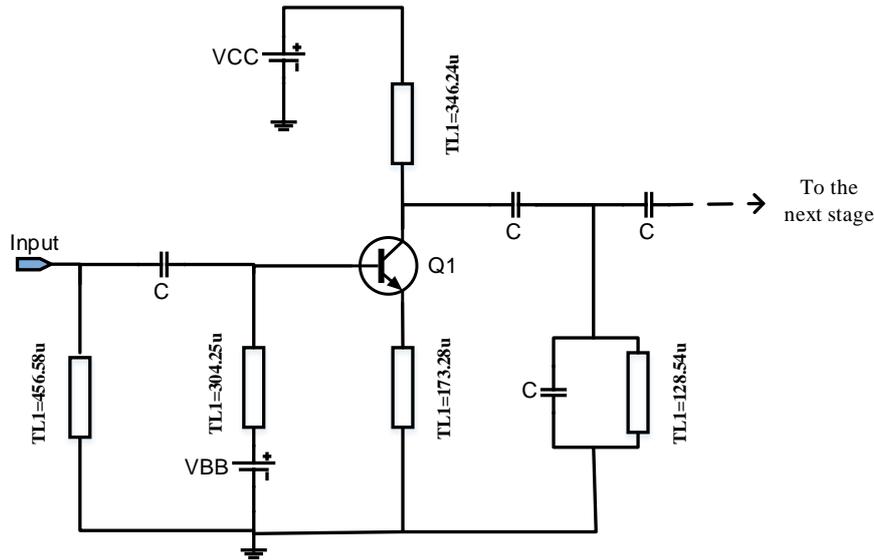
Figure 15: Unit cell of the three stages PA using microstrip transmission lines.

DESIGN THREE-STAGES PA USING TRANSMISSION LINES

The PDK provided by IHP foundry does not support optimization property in the ADS optimization tool, therefore, in the previous section ideal components have been used for design and simulation of a three stages PA shown in Figure 10. Thereafter, transmission lines and MIM capacitor models are used for design and simulation the same three stages PA. Figure 15 shows schematic circuit of the PA unit cell with lengths of microstrip transmission lines.

The parameters of microstrip transmission line can be extracted from an inductor as follows:

The input impedance of a shorted inductor can be calculated as [23]:

$$Z_{Ind} = j\omega L \qquad (8)$$

While, the impedance of terminated transmission line is:

$$Z_{Tl} = Z_0 \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)} \qquad (9)$$

Considering the case of shorted transmission line $Z_L = 0$, then,

$$Z_{Tl} = jZ_0 \tan(\beta l) \qquad (10)$$

By equating the two equations (8) and (10):

$$j\omega L = jZ_0 \tan(\beta l) \qquad (11)$$

The electrical length θ° can be calculated as:

$$\beta l = \theta = (2 \times \pi \times f \times L) \qquad (12)$$

While, the length of transmission line l (μm) can be calculated from equation (12) as:

$$l(\mu m) = tan^{-1}[(2 \times \pi \times f \times L/Z_0)] \times \frac{c}{2 \times \pi \times f \times \sqrt{\varepsilon_{eff}}} \qquad (13)$$

Where, $\beta l = \frac{2\pi}{\lambda_g} * l$, $\lambda_g = \frac{\lambda_0}{\sqrt{\varepsilon_{eff}}}$, and $\lambda_0 = \frac{c}{f}$. As well as β, λ_g, λ_0, ε_{eff}, C, and f are phase constant, effective wavelength, wavelength in vacuum, effective permittivity, speed of light, and frequency respectively.

The width w (μm) and characteristic impedance Z_0 (Ω) of microstrip transmission line can be calculated by the following formulas [23]:

When $w/h \leq 1$ the following equations are suitable for calculation:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + \frac{12h}{w}\right)^{-1/2} + 0.04\left(1 - \frac{w}{h}\right)^2\right] \qquad (14)$$

$$Z_0 = 60(\varepsilon_{eff})^{-1/2} ln\left(\frac{8h}{w} + \frac{0.25w}{h}\right) \Omega \qquad (15)$$

When $w/h \geq 1$ the following equations are suitable for calculation:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + \frac{12h}{w}\right)^{-1/2}\right] \qquad (16)$$

$$Z_0 = \frac{\left[120\pi(\varepsilon_{eff})^{-1/2}\right]}{(w/h) + 1.393 + 0.667 \ln(2.444 + w/h)} \Omega \qquad (17)$$

Where, ε_r, w, and h, are permittivity, width of transmission line, and substrate thickness, respectively. Figure 16, shows the length of transmission line, corresponding inductance for different width of transmission line.
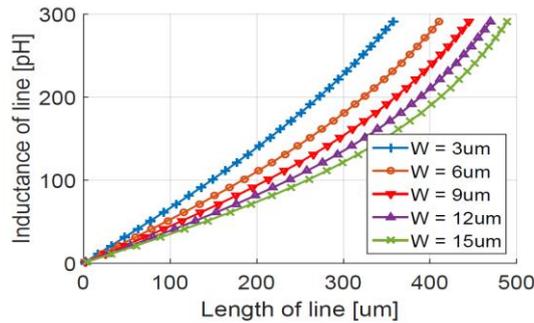
Figure 16: Relationship between inductance (pH) and length of microstrip transmission line (um) with variable width, at 60 GHz, ε_r=4.10, and h = 4.97 um.

The performance of three stages PA using transmission lines shown is in Figure 17, the reflections S_{11}, and S_{22} are greater than -10 dB at frequency band (50 – 65 GHz), while gain, PAE, and efficiency, are 14.4, 20.7%, 20.7%, respectively. Figure 18, shows the P_{sat}, and 1_{dB} compression are 6.5, and 4.5 dBm.
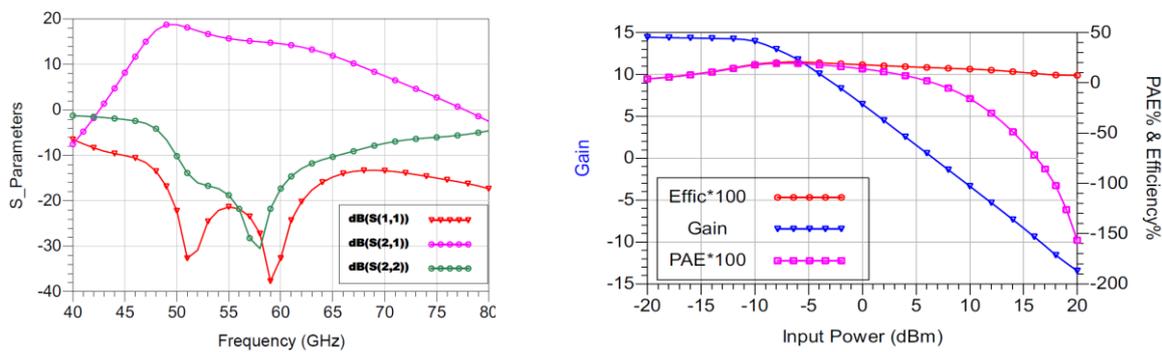
Figure 17: Small-signal S-parameters (left), and large-signal behavior (right) for the three stages PA using transmission line.
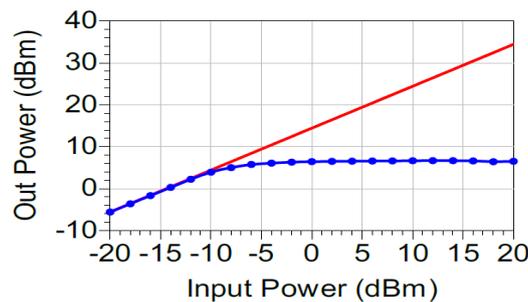
Figure 18: P_{sat}, and 1_{dB} compression for the three stages PA using transmission line.

The PA device can be unconditionally stable if K factor > 1, as well as Δ < 1 [24].

Where, $K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} > 1$ (18)

And, $|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1$ (19)

In addition, the μ factor for unconditional stability test is preferred in the case of compression between stability of two or more devices. Where

$\mu = \frac{1-|S_{11}|^2}{|S_{22}-\Delta S_{11}^*|+|S_{12}S_{21}|} > 1$ (20)

Figure 19 shows unconditional stability test for the three stage PA using transmission lines. If $\mu > 1$ the PA is unconditionally stable, and the greater value of μ indicates more stability as shown in Figure 19(a) around 60 GHz.
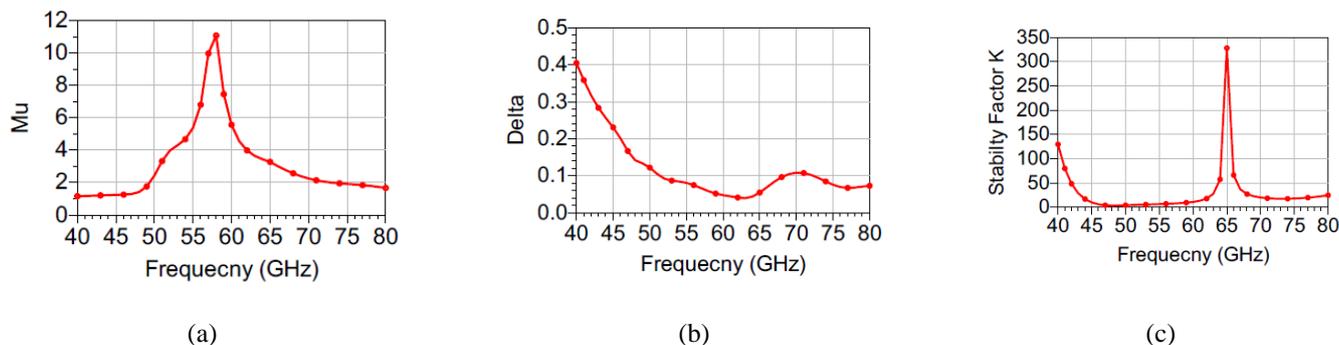
Figure 19: Unconditionally stability test for the three stages PA, (a) μ factor (b), Δ factor (c), and K factor.

CONCLUSION

In this paper, the design and performance optimization of a three stage 130nm SiGe PA was presented. A simple systematic way was used for the design and simulation of the PA. Firstly, the performance of single stage with variable number of emitter fingers (e.g. 3, 6, 8, 12, and 16) were investigated. Thereafter, the performance of single stage PA with six fingers was optimized and used as a unit cell for designing three stages PA. In addition, the input, output, and inter-stage impedance matching were optimized using ideal lumped components, then the ideal components were replaced by MIM capacitors and transmission lines, the final design has a reflections S_{11}, and S_{22} >-10 dB at frequency band (50 − 65 GHz), while gain, PAE, and efficiency, are 14.4, 20.7%, 20.7%, respectively, with good unconditionally stability. In future, the design can be validated with 3D full electromagnetic simulator to be ready for implementation.

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