A New Boost Converter with Edge Resonant Switched Capacitor

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Abstract- This paper presents a new soft switching PWM non-isolated boost DC-DC converter embedding an edge resonant switched capacitor (ER-SWC) modular. The soft switching PWM boost DC-DC converter treated here can achieve a high frequency zero current switching (ZCS) turn-on and zero voltage switching (ZVS) turn-off operations in active switches and minimize a reverse recovering current in the freewheeling diode under DCM including critical conduction mode (CRM) conditions in the input inductor current. Those advantageous properties enable a wide range of soft switching operations together with a high step-up voltage conversion ratio due to the edge resonance in the ER-SWC modular, which results in the high efficiency power conversion. For demonstrating the effectiveness of the new soft switching PWM boost DC-DC converter, a 1kW-40kHz laboratory prototype is evaluated in experiments, followed by the design guideline of the DC-DC converter and a theoretical analysis. Then, the performances of the proposed soft switching PWM boost DC-DC converter are discussed from a practical point of view.

Keywords: Boost DC-DC Converter; Edge Resonant Switched Capacitor; zero current switching.

1. INTRODUCTION

Recently there are many efforts to develop an efficient switch mode DC-DC converter for utility interfacing clean energy sources such as fuel cells, PV panels, super-capacitor banks and so forth. Development of boost DC-DC converters with new control strategies is coming up to increase the power processing capability and to improve the reliability of the power electronics system [1-5]. With the increasing demand for renewable energy, distributed power generation systems including solar PV have been studied and developed as a future energy source. For this system, a power conversion circuit is necessary to interface the generated power to the utility. In many cases, a high step-up DC/DC converter is needed to boost low input voltage to high voltage output. Conventional methods using cascade DC/DC converters cause extra complexity and excessive cost. The conventional topologies to get high output voltage use flyback DC/DC converters. They have leakage components that cause stress on the active switch and loss of energy resulting in low efficiency.

Several high voltage gain topologies were already proposed and a comparison of available topologies was done [6]. A high step-up coupled inductor boost-flyback converter was proposed before [7]. When higher output voltage is required, the multi-flyback converters are series connected. Diodes and capacitors with low rated voltage are used to improve the efficiency. A soft-switching boost converter for a PV generation system was proposed [8] using an auxiliary resonant circuit. The latter is composed of an auxiliary switch, a diode, a resonant inductor, and a resonant capacitor. It has better efficiency than a conventional boost converter even with the use of auxiliary switches and complicated control circuit with a subsequent increase of the conduction and switching losses. This reflects itself on the increase of the cost and size of the converter. DC–DC converters are frequently paralleled to reduce output ripple and an interleaved boost converter was proposed [9].

The simplest boost converter is as shown in Fig. 1-a). A circuit composed of two coupled inductors was introduced [6] as illustrated in Fig. 1-b), with high utilization grade of the magnetic core. Depending on the turns-ratio between the inductors, the voltage stress across the active switch can be as low as 15% of the output voltage. Like other topologies requiring coupled inductors, the high turns-ratio between windings increases system complexity and losses. A simplified variation was also proposed [10, 11] with three coupled inductors, Fig. 1-c) though their leakage inductance may lead to a ringing phenomenon in the voltage across diode D2. A hybrid boost-flyback converter was proposed [7] with the advantage of low voltage stress across the active switch, which is equal or lower than half of the output voltage; depending on the turns-ratio between the windings. In addition, such voltage is naturally clamped by an output capacitor that additionally recycles the leakage energy to the output. As a disadvantage, the input current is pulsating and requires an additional input filter.

Another topology - similar to the previous one - consisting of a boost converter with coupled inductors was introduced [12] as is illustrated in Fig. 1-(d). In this figure, a voltage doubler rectifier is applied to the secondary winding. Drawbacks of this approach are the necessity of a filter to treat the input pulsating current. The proposed topology [13] as depicted in Fig. 1-(e) uses also coupled magnetic structures, though in a different way than previous approaches. Here, a three-state switching cell composed of two active and two passive

switches employs an autotransformer with equal number of turns and inversed polarity in order to provide balanced current share [14]. Coupled with such transformer is a secondary winding that allows simultaneously high voltage gain and reduction of voltage stress across active switches with variation of turns-ratio. The use of two active switches in parallel with reduced voltage rating allows the minimization of conduction losses. A further advantage is that the frequency across the inductor is double of the switching frequency; allowing reduction of the size and subsequently the switching losses. Finally, the input current is non-pulsating with little ripple, what leads to low maximum power point (MPPT) mismatches. The voltage level across the active switches is naturally clamped by the capacitor C1 in Fig. 1 (e). A higher number of active switches are necessary [15] with the increase of losses and control complexity.
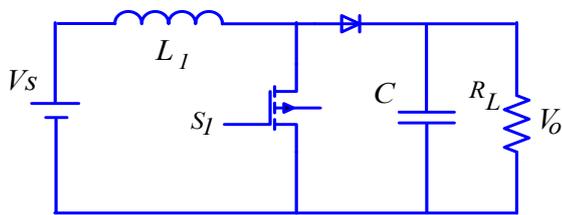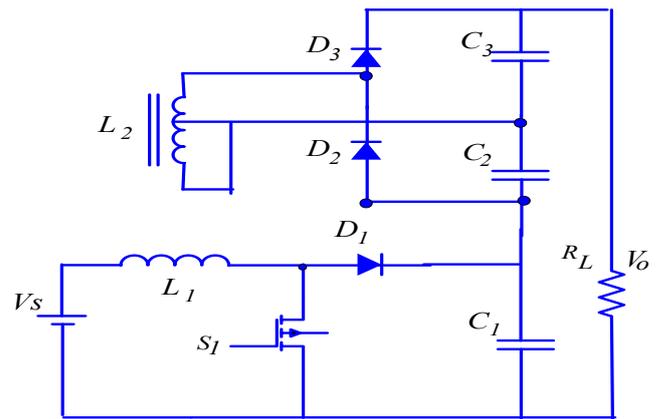

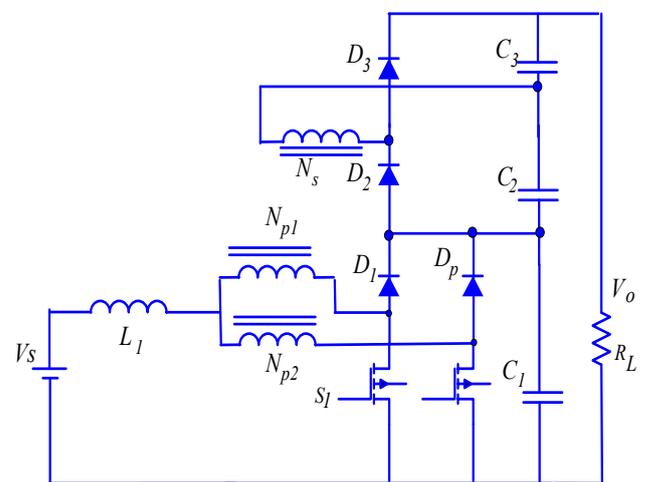a) Conventional type unidirectional boost DC-DC converter [16, 17]
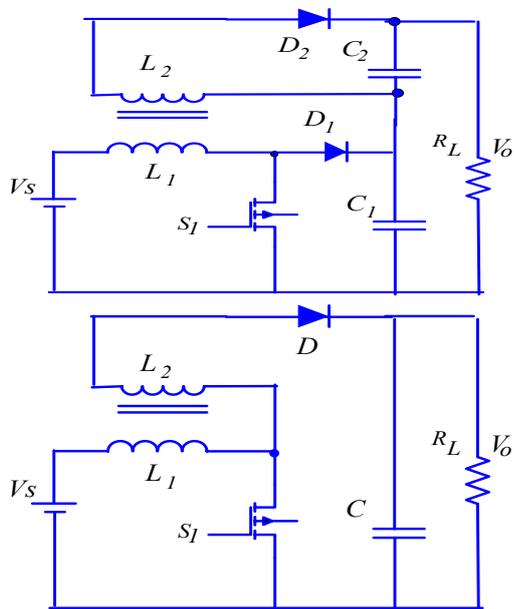
b) Boost converter with two coupled inductors [6]
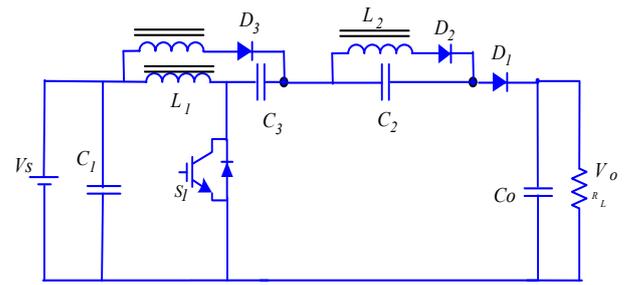
c) Boost converter with three coupled inductors [11]

d) Boost converter with coupled inductors and voltage doubler rectifier at the secondary winding [7].

e) Boost converter with two active switches and secondary voltage doubler rectifier [13].

Fig. 1 High gain DC-DC converter topologies

In particular, DC-DC power conversion employing taped inductor boost converters has several advantages [18], such as ripple cancellation in the waveform to maximum extent, lower value of ripple amplitude as well as high ripple frequency in the resulting input and output waveforms. Further, parallel connection of converters also reduces the maintenance,

increases the reliability and fault tolerance. Furthermore, the dual boost taped inductor approach for the DC-DC converters reduces the steady-state current ripple, conduction losses in the switching devices and core losses if proper core structure is employed. Dual boost converter for PV interface is simple with low cost topologies that give substantially high efficiencies even at low voltage and high currents. However, one has to optimize the output inductor and filter capacitor components to achieve desired transient and steady-state performance requirements for PV interface systems. To have faster dynamic response, the boost inductors have to be as low as possible [16]. On the other hand, the low inductance value increases the output voltage ripple, thus deteriorating the steady-state performance. A tapped inductor buck converter was proposed [18] for voltage regulator modules. The tapped inductor in the output filter of the DC-DC converter was used [19].

Several controlling methods, including voltage mode, current mode and hysteretic control are proposed [20-23]. Each of these methods has its own advantages. The boost converter can operate in two different modes depending upon its energy storage capacity and the relative length of the switching period. These two modes are known as continuous and discontinuous conduction modes.

This paper presents a novel circuit topology for boost DC-DC converter interfacing PV systems. The configuration of the proposed circuit is described in the next section (section 2). The load for the boost stage is the battery and the forward converter stage of the inverter system behaves more like a constant power load rather than a resistive load. Based on the load conditions, the boost stage can be controlled to draw a specific amount of current determined by the size of the inductor, and duty ratio. The converter in continuous and discontinuous conduction modes is also analyzed.

In section 2, the well known simulation program PSIM is used to model the PV and simulate the closed loop converter system. The control strategy is discussed. Steady state response analysis and other simulation studies are discussed. Section 3 explains the operation principle using the switching modes equivalent circuit and operation waveforms. Then, the analysis of continuous and discontinuous conduction modes is presented in sections 4 and 5.. Section 6 presents calculations of losses and efficiency of the proposed converter. Section 7 presents the experimental results of a prototype dual boost converter. Output voltages and currents were measured at a number of power levels.

2. CIRCUIT CONFIGURATION

The circuit configuration of the proposed soft switching PWM boost DC-DC converter is illustrated in Fig. 2. The Edge-Resonant Switched Capacitor (ER-SWC) modular consists of two active switches $S1$, $S2$, two auxiliary diodes $D1$, $D2$, a resonant capacitor Cr and a resonant inductor Lr. The circuit arrangement of the proposed ER-SWC modular can be modified for the other types of topologies as depicted in Fig. 1, and all of them can be applied for the six non-isolated

PWM DC-DC converters (Buck, Boost, Buck-Boost, Cuk, SEPIC, Zeta) [6].

The key advantages of the proposed soft switching PWM boost DC-DC converter are summarized as follows:

High step-up voltage conversion ratio can be attained due to the DCM and edge resonance by Lr and Cr.

- ER-SWC modular is configurable by CMOS circuit structure and H-bridge module.

- Current sharing operation is available between $S1$ and $S2$, which is effective for applications with a large input current.

- The gate signal for $S1$ and $S2$ can be common, so the gate drive circuits are comparatively simple than the conventional converter.
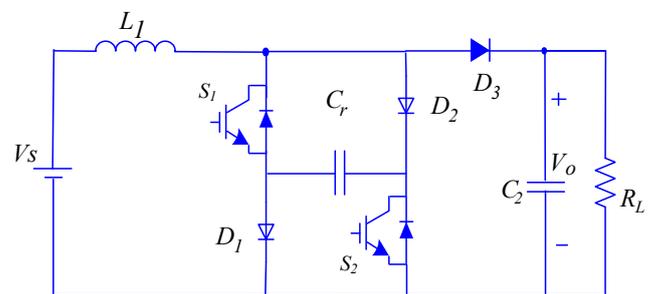
Fig. 2 Proposed soft-switching boost DC/DC converter

3. PRINCIPLE OF OPERATION

During one commutation period of the converter operation, it presents four operating intervals that are described in this section 3. The equivalent circuits of operation intervals of the proposed one stage high frequency dual boost converter during one switching cycle are shown in Fig. 3. The corresponding operating voltage and current waveforms are shown in Fig. 4. Four operating intervals take place during one switching period. Fig. 5 shows diodes current and inductor current. Fig. 6 shows output voltage and current of proposed DC-DC converter

The operation principle of the converter is explained in the following by using the corresponding switching interval equivalent circuits:

Interval 1 (SW_1: ON, D_1, D_2 and D_3: ON); $0 \le t < t_1$.

S_2 ZCS turn-on mode: The inductor current i_{Lr} is zero, and the active switches S_1 and S_2 are simultaneously turned on at t_0. Then, i_{Lr} and the switch currents i_{S1} and i_{S2} rise gradually from the zero initial value with the edge resonance by L_r and C_r. Thereby, ZCS turn-on commutation can be achieved in S_1 and S_2. During this mode, i_{Lr} is written by:

$$i_{Lr} = \frac{V_{in} + V_o}{Z_r} \sin \omega_r (t - t_o)$$ (1)

where $Z_r = \sqrt{L_r / C_r}$ and $\omega_r = \sqrt{L_r C_r}$.

The inductor current i_{Lr} at $t=t_1$ can be obtained by

$$I_{Lr1} = i_{Lr}(t_1) = \frac{\sqrt{V_o(2V_{in} + V_o)}}{Z_r} \qquad (2)$$

$$t_1 = \frac{1}{\omega_r} \cos^{-1} \frac{V_{in}}{V_{in} + V_o} \qquad (3)$$

The resonant capacitor Cr is discharged by the edge resonant current in the ER-SWC modular in this interval.

Interval 2 (S_1: ON, D_1, D_2 and D_3: ON); $t_1 \le t < t_2$.

inductive energy storing mode: The resonant capacitor Cr is completely discharged at $t1$, then the diodes $D1$ and $D2$ are forward biased. During this interval, iLr rises linearly as expressed by:

$$i_{Lr} = \frac{V_{in}}{L_r}(t - t_1) + I_{Lr1} \qquad (4)$$

The inductor current iLr is equally shared by the two branches $S1–D2$ and $S2–D1$. From (4), iLr at $t2$ can be determined by:

$$I_{Lr2} = i_{Lr}(t_2) = \frac{V_{in}}{L_r}(DT - t_1) + I_{Lr1} \qquad (5)$$

where D denotes the duty cycle and S1 and S2, and it can be defined by

$$D = T_{on}/T \qquad (6)$$

Interval 3 (SW_1: ON, D_1, D_2 and D_3: ON); $t_2 \le t < t_3$.

$S1$, $S2$ ZVS turn-off mode: The two active switches $S1$ and $S2$ are turned off simultaneously at $t2$. Then, edge resonance begins again in the ERSWC modular, and the voltages across $S1$ and $S2$ increase gradually by the effect of Cr. Thereby, ZVS turn-off commutation can be achieved in $S1$ and $S2$. During this mode, iLr is defined by:

$$i_{Lr} = I_{max} \sin\left\{\omega_r(t - DT) + \tan^{-1}\frac{Z_r I_{Lr2}}{V_{in}}\right\} \qquad (7)$$

where I_{max} represents the peak value of i_{Lr}, as expressed by

$$I_{max} = \sqrt{I_{Lr2}^2 + \left(\frac{V_{in}}{Z_r}\right)^2} \qquad (8)$$

This operation mode continues until the capacitor voltage vCr equals to the output voltage Vo at $t3$, and the corresponding inductor current can be defined by:

$$I_{Lr3} = i_{Lr}(t_3) = \sqrt{I_{max}^2 - \left(\frac{V_o - V_{in}}{Z_r}\right)^2} \qquad (9)$$

$$t_3 = \frac{1}{\omega_r}\left(\sin^{-1}\frac{V_o - V_{in}}{Z_r I_{max}} + \tan^{-1}\frac{V_{in}}{Z_r I_{Lr2}}\right) + DT \quad (10)$$

Interval 4 ($t3 \le t \le t4$) inductive energy releasing mode:

The resonant capacitor voltage vCr rises up to the output voltage at $t3$, then the conduction interval of $D1$ and $D2$ are terminated. The inductor current iLr is forward to the load via Do, and thereby the input voltage Vin is boosted to the output voltage Vo. During this interval, iLr is expressed by:

$$i_{Lr}(t_4) = \frac{V_{in} - V_o}{L_r}(t - t_3) + I_{Lr3} \qquad (11)$$

$$t_4 = t_3 + \frac{L_r I_{Lr3}}{V_o - V_{in}} \qquad (12)$$

Thereby, occurrence of the reverse recovering current can be mitigated for the output freewheeling diode Do.

Interval 5 ($t_4 \le t \le t_5$) inductor current discontinuous mode:

Inductor current i_{Lr} reduces to zero level after t_4, then the load current flows through the output capacitor C_o. The inductor current keeps zero until the next one cycle starts at t_5.
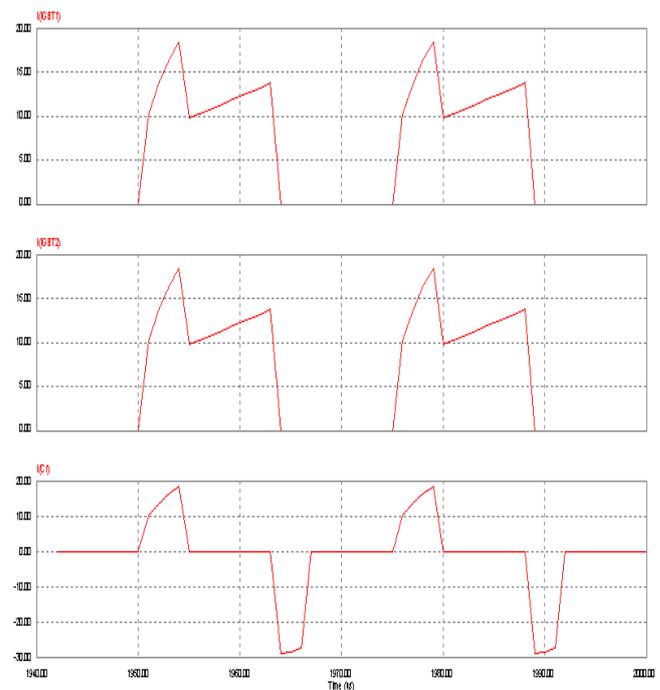

Fig. 4 Switches current and capacitor Cr current
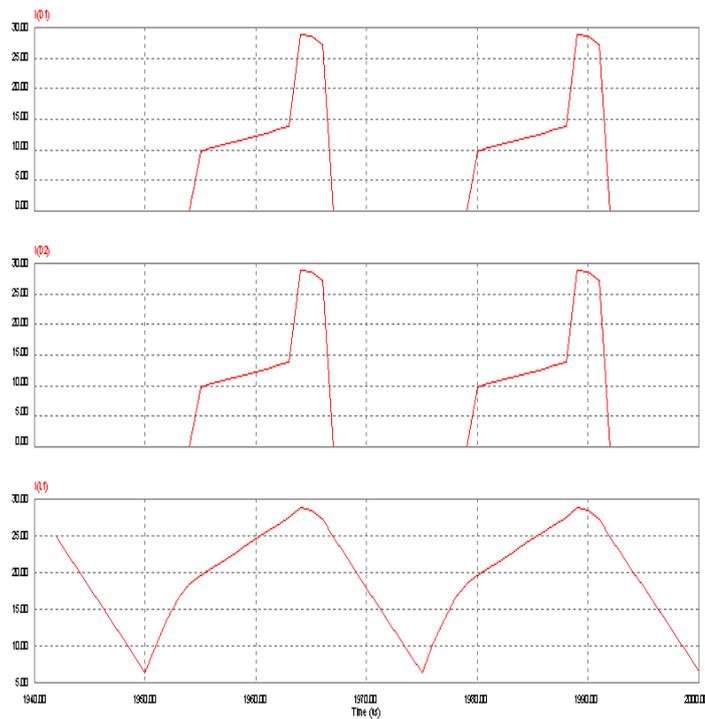
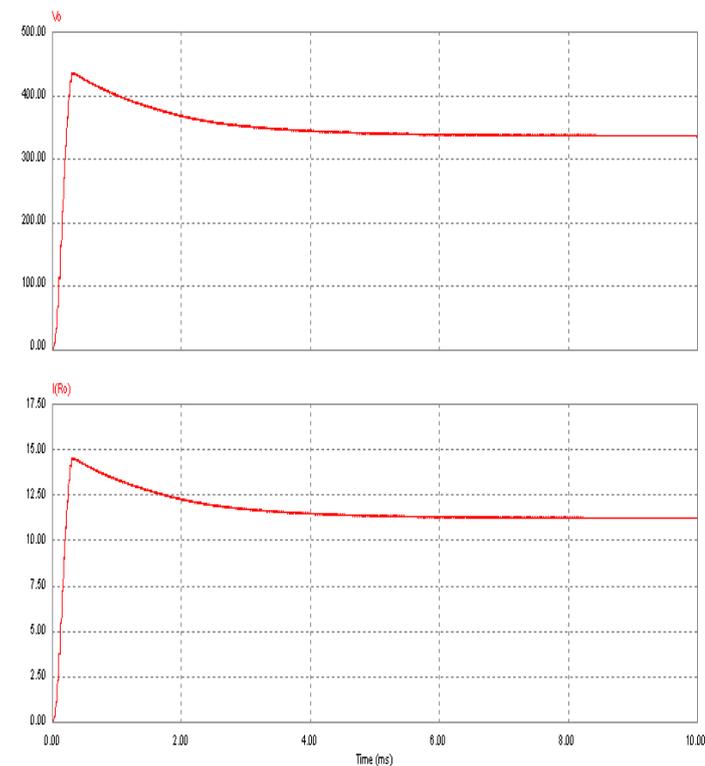**Fig. 5** Diodes current and inductor current

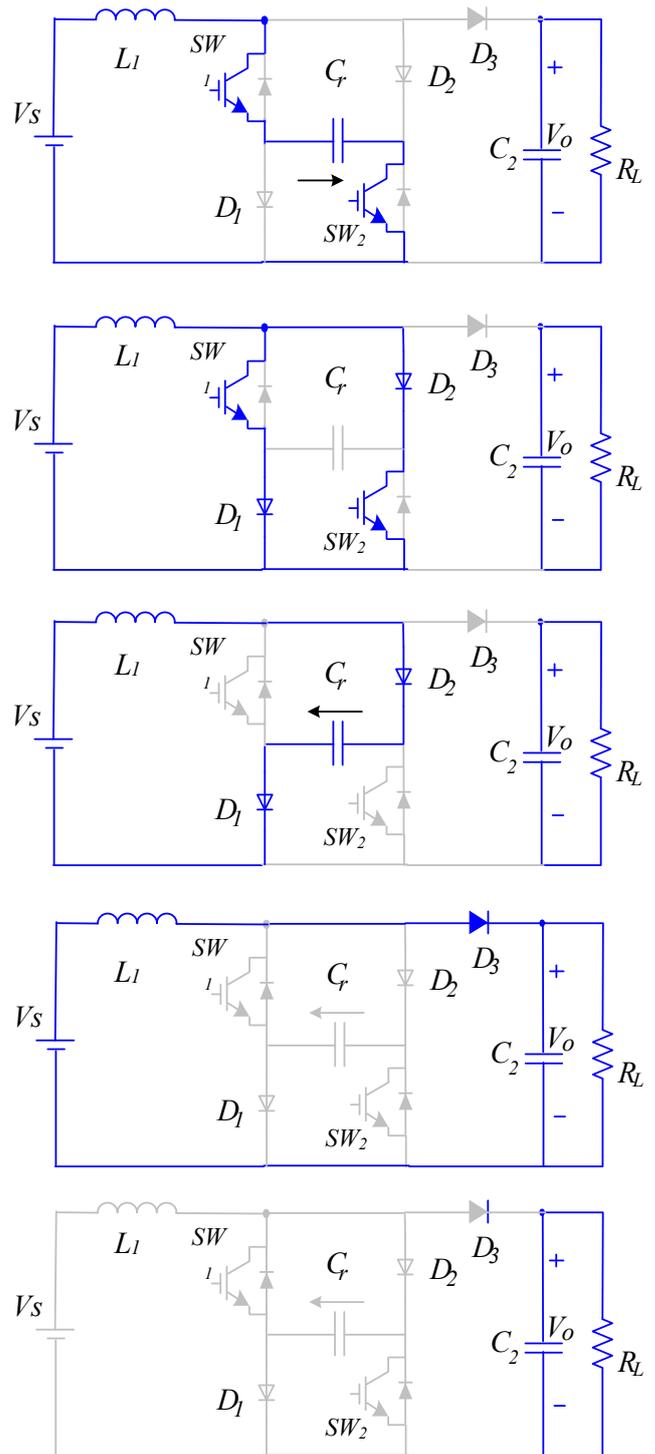**Fig. 6** Output voltage and current of proposed DC-DC converter

Fig. 7 Equivalent circuits of operation modes

4. CALCULATION OF CONVERTER LOSSES AND EFFICIENCY

A MATLAB script file was written to calculate the losses and thus efficiency of the proposed converter. The first step in calculating the losses was to calculate the RMS currents in the various components of the circuit [22]. For example, in the boost converter, the peak to peak inductor ripple current $i_{L\,(1)}$ along with the average inductor current which is the input

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current Ii is used to calculate the RMS inductor current (6). From this the RMS switch current I_{Qrms} (7) and RMS diode current $I_{D1\text{-}rms}$ (8) can be calculated given the respective duty cycles D and (1-D) of these devices. The input and output capacitor RMS currents $I_{C1\text{-}rms}$ (10) and $I_{C2\text{-}rms}$ (11) are the ac components of the input and output currents. For simplicity, these formulae all assume continuous conduction mode (CCM), which was true in this study to approximately 10% of the converters rated current. The minimum inductor current (5) is calculated to check for the boundary of CCM. Boost converter losses versus the input current in Fig. 8.

$$i_L = t_{on}\frac{V_i}{L} \tag{13}$$

$$I_{L\min} = I_i - \frac{i_L}{2} \tag{14}$$

$$I_{Lrms} = \sqrt{I_i^2 + \frac{i_L^2}{12}} \tag{15}$$

$$I_{Qrms} = \sqrt{I_{Lrms}^2 D} \tag{16}$$

$$I_{Drms} = \sqrt{I_{Lrms}^2(1-D)} \tag{17}$$

$$I_{D1-rms} = \sqrt{I_{L1-rms}^2(1-D)} \tag{18}$$

$$I_{Ci-rms} = \frac{i_L}{\sqrt{12}} \tag{19}$$

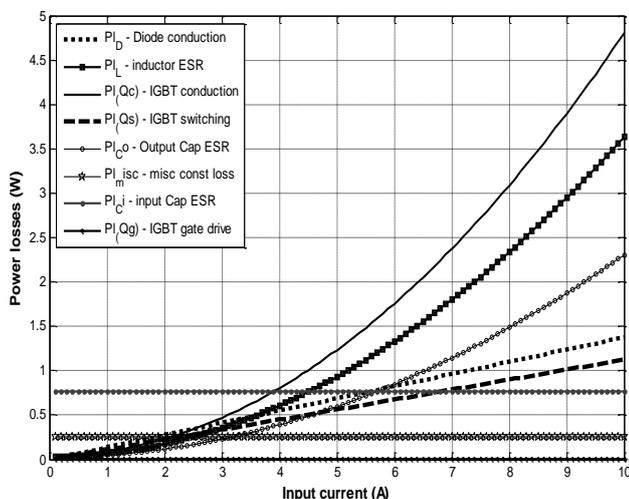$$I_{Co-rms} = \sqrt{I_{D-rms}^2 - I_o^2} \tag{20}$$

Fig. 8 Boost converter losses versus input current

5. CONTROL CIRCUIT

The approach used to track the MPP of the array was a perturb and observe (P&O) algorithm that is well suited to PIC microcontroller implementation. The P&O algorithms operate by periodically perturbing (i.e. incrementing or decrementing) the array terminal voltage or current and comparing the PV output power with that of the previous perturbation cycle. If the PV array operating voltage changes and power increases (dP/dV>0), the control system moves the PV array operating point in that direction; otherwise the operating point is moved in the opposite direction. To follow-up the change of insolation level and temperature, the perturbation cycle is repeated and the algorithm continues in the same way. The MPPT algorithm is embedded in the logic block and produces a reference voltage in order to adjust the duty ratio to move the operating point on the P-V characteristics of the PV array. The reference voltage is fed into a comparator and compared with a saw tooth waveform. Finally a PWM switching signal is generated to drive the switch SW1 and SW2 of Fig. 1. The output voltage is sensed to be controlled within the specified limits. The control system is given in a block diagram Fig. 9.

In Fig. 9, the adopted converter is controlled by PIC microprocessor used to implement an MPPT perturb and observe (P&O) algorithm.
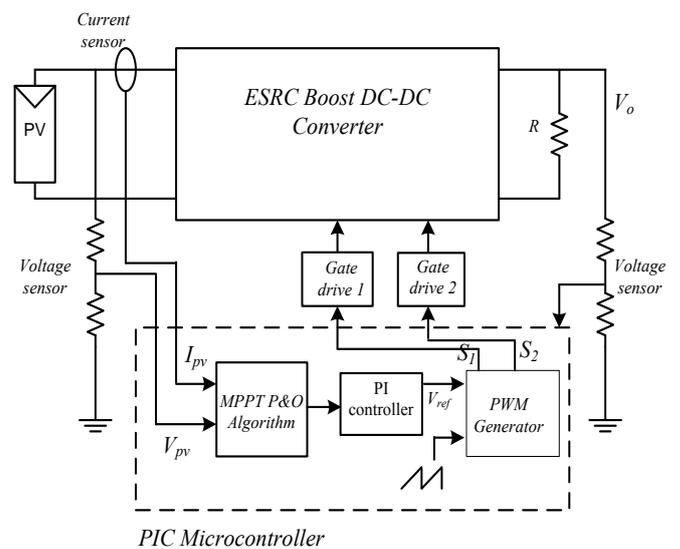

Fig. 9 Block diagram of the soft-switching boost converter

6. EXPERIMENTAL RESULTS

Fig. 10 and 11 shows the current and voltage waveforms of the upper arm switch and the auxiliary switch, respectively. As can be seen, the upper arm switch and the auxiliary switch turn on and turn off with zero currents, which reduce the switching losses.

TABLE I

Circuit parameters of laboratory prototype.

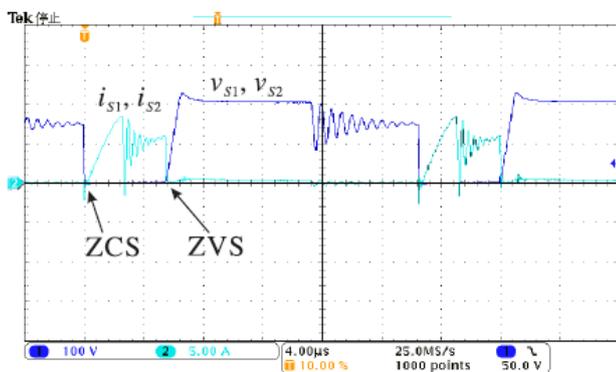| Parameter	Value [unit]
Power rating, P_o	1 [kW]
Input voltage, V_{in}	100 [V]
Output voltage, V_o	200 [V]
Resonant inductor, L_r	68 [μH]
Resonant capacitor, C_r	56 [nF]
Variable load resistor, R_o	40–400 [Ω]
Output side smoothing capacitor, C_o	1000 [μF]
Switching frequency, f_s	44 [kHz]

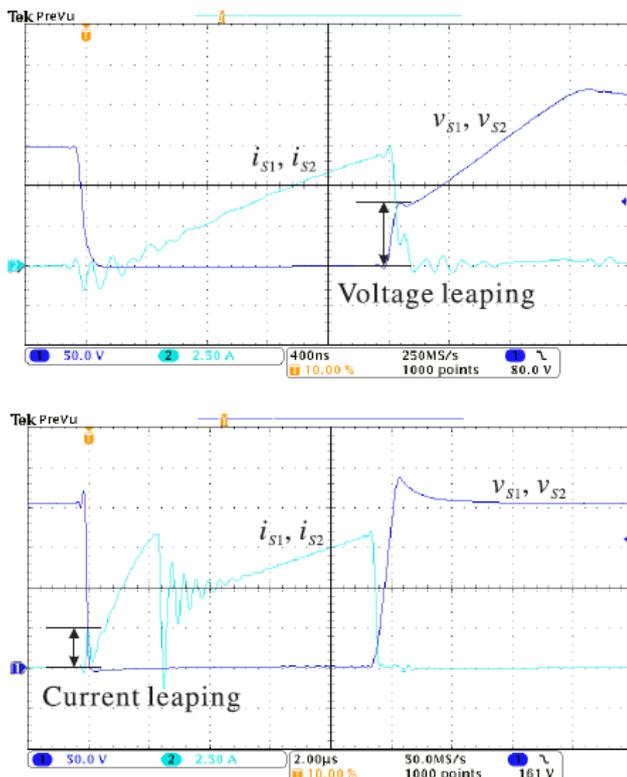**Fig. 10** Voltage and Current waveforms at P=500 W

Fig. 11 Voltage and Current waveforms of the switch S1

Fig. 12 shows the measured efficiency. Theoretically calculated efficiency of dual boost dc–dc converter is shown in Fig. 12. The proposed circuit has higher efficiency than the hard switching inverter. The maximum efficiency is 97.5 % at full load and about 2 % of improvement of the efficiency is obtained.
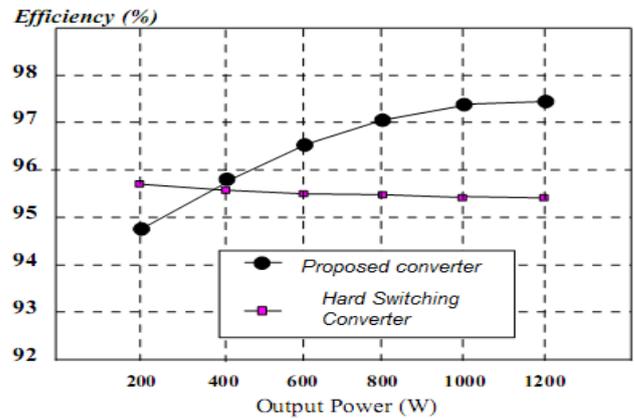

Fig. 12 Measured Efficiency, ttheoretically calculated efficiency of dual boost dc–dc converter.

CONCLUSIONS

- A new circuit topology of dual boost high voltage gain DC-DC converter has been presented.

- The proposed circuit has various advantages compared to the conventional boost converters; namely higher boost rate with low duty cycle, lower voltage stress on components and higher efficiency.

- The operation analysis was presented through operation modes and equivalent circuit of each mode.

- The control strategy is discussed for the proposed soft-switching boost DC-DC converter.

- Mathematical and theoretical analyses are presented along with selected simulation results to support the theoretical considerations.

- Losses and thus efficiency is calculated of the proposed converter.

- A PV system simulation model is developed using PSIM to validate the proposed converter

- Experimental results are reported to verify the proposed solutions using a prototype converter.

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