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Performance Evaluation of Low-Power 4 X 4 Bit Memory Array Multiplier

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Abstract

For any digital integrated chip the multipliers are the basic module needed for almost all arithmetic and logic unit (ALU) application. It is used right from small multiplier circuits to huge multiprocessor design, hence since its uses are vast so the design needs to be very efficient with respect to its desired operation and also it should be capable for low power and high speed operation. This paper presents 4X4 bit binary multiplier which uses half and full adder as its circuit subsystems and to maintain low power and high speed the gate diffusion input (GDI) cells are used. The result shows the low power and high speed operation of the 4 X 4 bit binary multiplier as the proposed design consumes approximately 9µW power with the propagation delay of nearly 18ns.

Keywords: Multiplier, GDI Cell, Low Power, Partial Products, MOS Characteristics.

I. INTRODUCTION

A "P X Q" multiplier can be considered as "P + Q" inputs and "P + Q" outputs as well. This device performed P bits X Q bits multiplication as shown in figure – 1(a) below. The block diagram is also shown in the figure – 1(b).

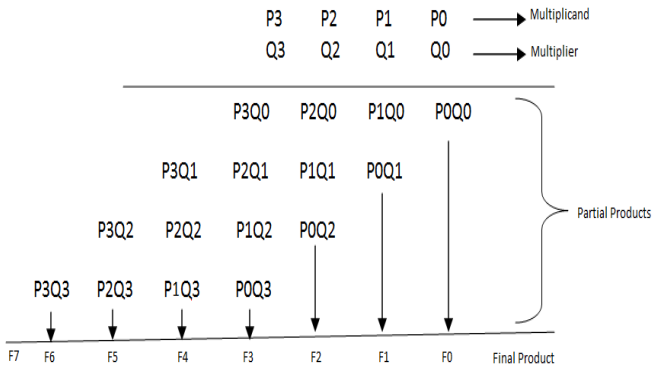

Figure 1(a): 4 X 4 Bit Multiplication Operation

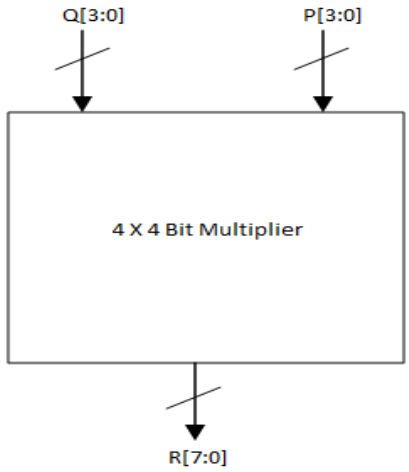

Figure – 1(b): 4 X 4 Bit Multiplier Symbol

Here the multiplication process consist of four multiplicand bits P0, P1, P2, and P3 and four multiplier bits Q0, Q1, Q2, and Q3, partial products bits and eight finally product bits. Using AND gate the partial products are generated; and the partial product bits and the carries between the stages are indicated by XOR operation. The below calculation Shows the summation of partial products and carries required to produce the product bits for the 4 X 4 bit multiplier.

F0 = P0Q0

F1 = P1Q0 xor P0Q1

F2 = P2Q0 xor P1Q1 xor P0Q2

F3 = P3Q0 xor P2Q1 xor P1Q2 xor P0Q3

F4 = P3Q1 xor P2Q2 xor P1Q3

F5 = P3Q2 xor P2Q3

F6 =P3Q3

F7 = Last Carry (As per the operation)

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To perform the multiplication operation the partial products are generated first using AND gates as shown in figure – 1(c).

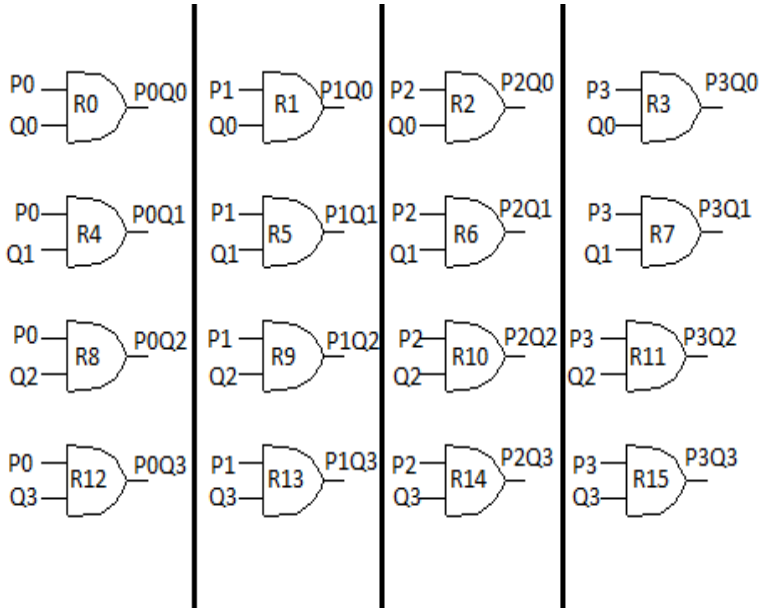

Figure 1(c): Partial Product Generation

II. PROPOSED MODEL

The proposed 4 X 4 bit binary multiplier is shown in figure – 2(a); it consists of nine full adder and three half adder. The 4 X 4 bit binary multiplier is design hierarchically, that is first the AND & XOR gate is designed using GDI technique, the GDI cell for AND & XOR is shown in figure – 2(b).

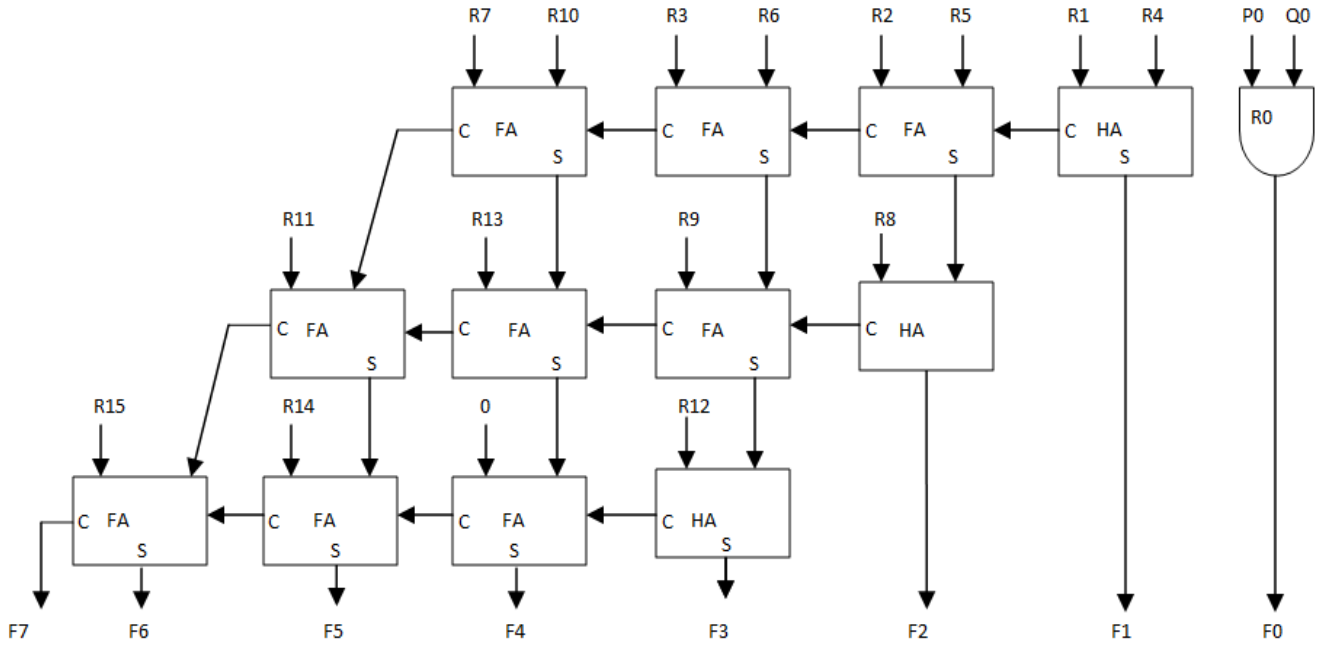

Figure 2(a): 4 X 4 Bit Binary Multiplier

About GDI Cell: - The gate diffusion input (GDI) technique is a design methodology for low power digital circuits and systems. This technique helps in reducing propagation delay, power consumption, and also area of the digital circuits. Furthermore it also reduces the complexity of design the cell for digital circuits as less number of transistors are required as compared to conventional CMOS and transmission gate design technique. This overall results in less complex layout of the circuit which is very critical part of the IC design. The proposed 4 X 4 Bit multiplier uses this GDI technique to design the various blocks and sub-blocks at transistor level and then use them as a main circuit sub systems.

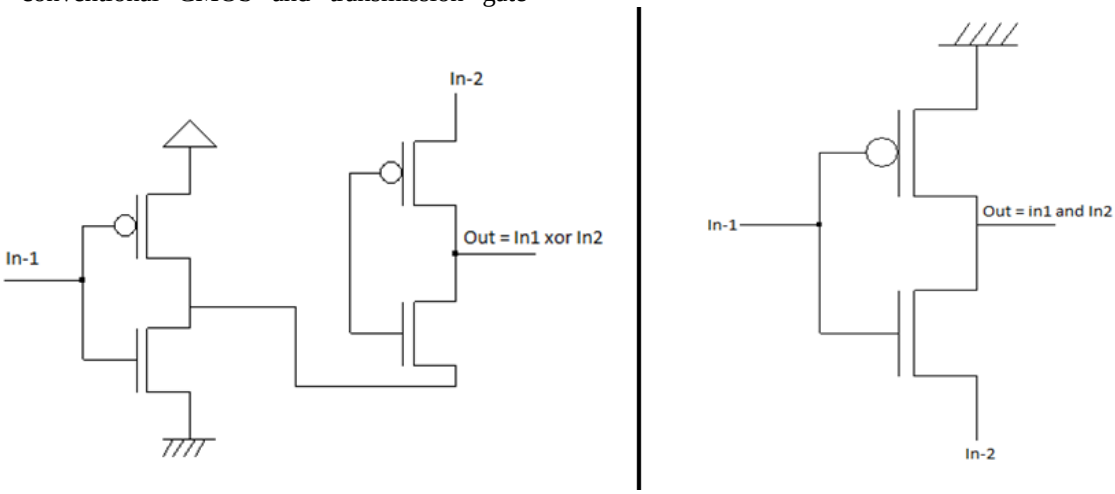

Figure 2(b): GDI Cell of AND & XOR Gate

Table 1: Simulation Conditions

Device Name	**MOS Size (W/L)**
PMOS	350/32
NMOS	150/32
Supply and other Inputs	
VDD	3.2V DC
Inputs (all combinations)	P[3:0] (0000 to 1111) , Q[3:0] (0000 to 1111)
Model File	32nm Standard Process Technology

III. SIMULATIONS AND RESULTS

The HSPICE simulator is used for simulating the proposed model and the process technology is chosen as standard 32nm. The functionality of the 4 X 4 bit binary multiplier is verified by writing HDL code. The various parameters related to the simulation are listed in above Table – 1.

The below figure – 3(a, b, and c) shows the relations between Ids vs. Vgs, Ids vs. Vgs and the parasitic capacitances. These values are computed using Level – 1, Level – 3, and BSIM models. The results are listed in Table – 2. The result shows the proper operation of 4 x 4 bit binary multiplier, and the behavior of various signal involved in the design are shown below. The figure – 3(d) below shows the HDL model of 4 x 4 bit binary multiplier and it can be seen that the proposed model is working as expected. The optimized layout is shown in figure – 3(e)

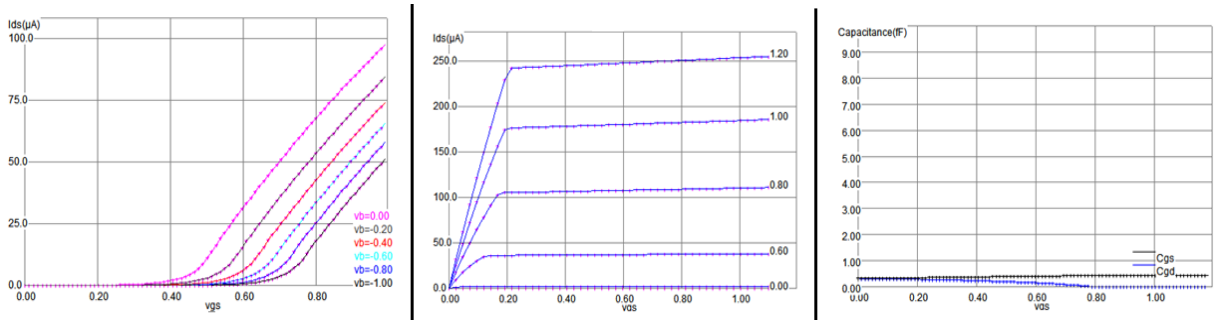

Figure 3(a): Relations w.r.t Level – 1

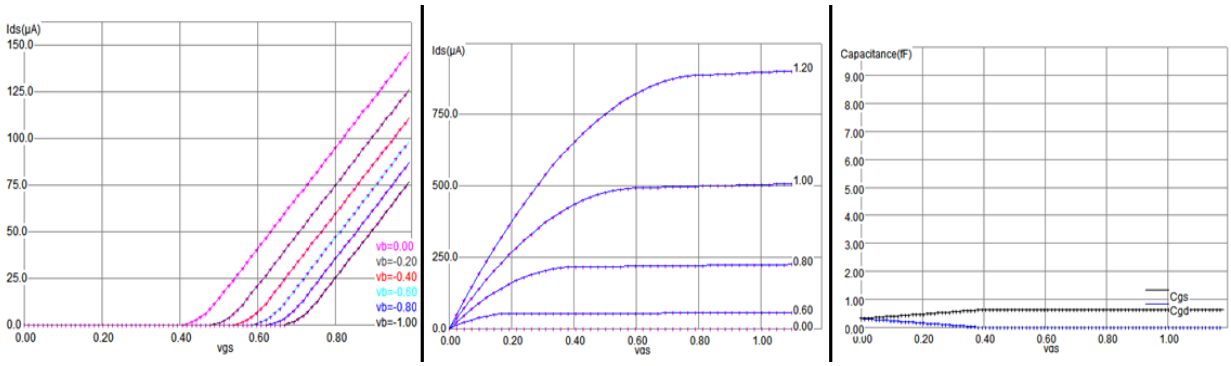

Figure 3(b): Relations w.r.t Level – 3

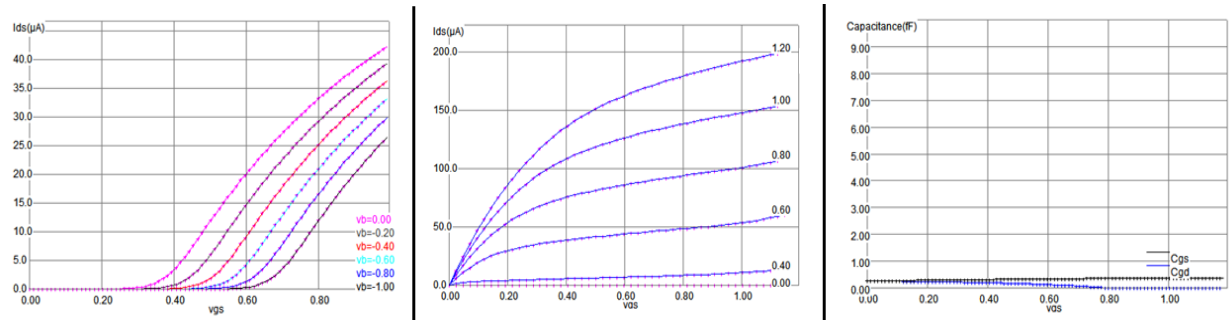

Figure 3(c): Relations w.r.t BSIM models

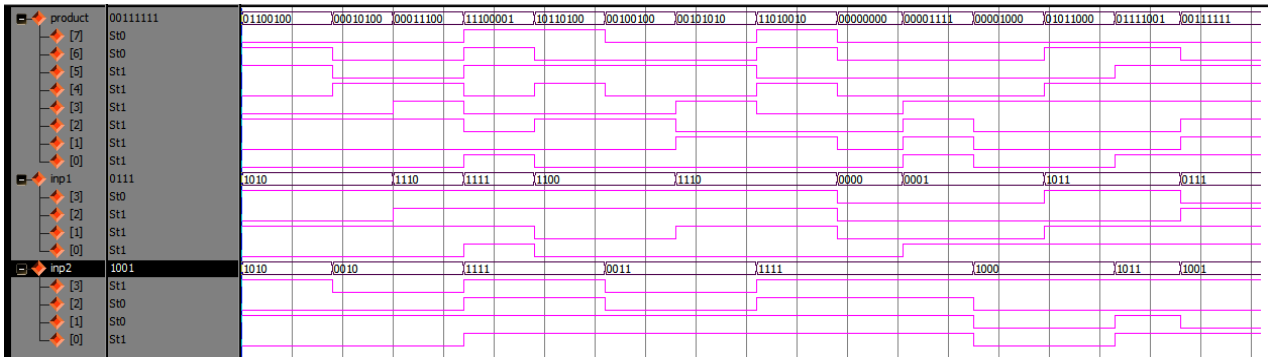

Figure 3(d): HDL verification of 4 X 4 Bit Binary Multiplier

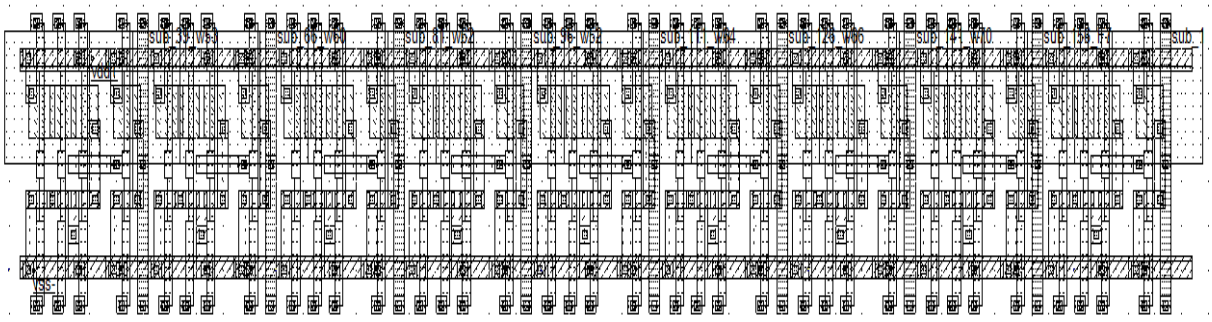

Figure 3(e): Layout of 4 X 4 Bit Binary Multiplier

Table 2: Simulation Results

Parameters	**Values**
Total Average Power	8.37 µW
Cgd (Average)	1.59 fF
Cgs (Average)	1.82 fF
Propagation Delay	18.3 ns
Area Optimized (Using GDI Cell)	34%

IV. CONCLUSION

This paper presents 4 x 4 bit binary multiplier and its working. The multiplier is designed using optimized process parameters and it is observed that the 4 x 4 bit binary multiplier performs as it should and due to use of GDI cell it consumes very less power as compared to conventional CMOS. The results also reveal that the GDI cell requires less area as compared to conventional CMOS. The propagation delay also reduces in the design of half and full adders using GDI cell which helps in reducing overall delay of the multiplication operation of the 4 X 4 bit binary multiplier circuit.

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