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Power Losses Balancing in Full-Bridge Submodule of Modular Multilevel Converter

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ABSTRACT:

Full bridge MMC submodule thermal modes of operation are considered. A number of pulse width modulation modifications for power losses balancing by means of zero states redundancy utilization are compared for the particular design of modular multilevel converter based active power conditioner with uninterruptible power supply capability. It is shown that proposed method of PWM modification yields to 8.6 ^{0}C reduction of the highest pn-junction temperature while total losses of submodule increase less then 1%.

Keywords: Thermal mode, Power losses, Balancing, Submodule, PWM, MMC, IGBT.

I. INTRODUCTION

Modular multilevel converter scheme was proposed by Professor R. Marquardt in early 2000s [1]. For the past 15 years MMC technology was extensively used for HVDC transmissions, HVDC B2B and STATCOM equipment [2]. MMC control, design and other related areas are still developing although a number of MMC based projects are commissioned at present.

IGBT-module thermal modes optimisation is one of critical problems in MMC submodule design so investigations is this field are conducting worldwide. Relevant paper analysis showed that some PWM modifications are proposed [3] for power losses balancing among submodules of MMC arm. Another work [4] presents simplified method of thermal modeling for IGBT modules with periodic power losses in MMC. Both [3] and [4] consider half-bridge submodule. While electro-thermal design of a MMC prototype incorporating full-bridge is presented in [5].

This article discovers problem of optimal zero state redundancy utilization for power losses balancing and temperature balancing among power semiconductor devices located in one submodule. These aspects are considered on particular example, namely on MMC based active power conditioner with uninterruptible power supply capability [6].

This paper is organized as follows. Basic MMC design parameters developed in project and submodule scheme are presented in Section 2. Electrical modes of developed converter are described in Section 3. PWM notes are given in Section 4. Electrical and thermal model used for analyses are described in Section 5. Gained computer modeling results are illustrated is Section 6 and some conclusions are given in Section 7.

II. CONVERTER DESIGN

Converter scheme shown in Fig.1a was developed for modular multilevel converter based active power conditioner with uninterruptible power supply capability [6]. Main converter parameters are indicated in Table 1. Discussed device contains voltage source converter and supercapacitor based energy storage. The converter includes six arms grouped into three phases. Each arm includes reactor and a number of identical submodules connected in series.

Table 1. Power Conditioner Specifications

Parameter	Value
Rated AC Voltage	6.0 kV
Rated power	6.0 MVA
Number of submodules in arm	10
Rated SM voltage	1200 V
Rated energy storage capacity	9.0 MJ
Rated DC voltage of energy storage	9.6 kV
Peak active power	3.0 MW
PWM switching frequency	1000 Hz
Arm reactor inductance	5.0 mH

Most of the time described power conditioner acts as active filter compensating imaginary power of load connected in parallel with it. Power conditioner starts to supply active power to sensitive load during deep voltage sag, momentary or instantaneous interruption after islanding them from the main grid.

Simplified scheme of full FB-SM power circuit is shown in Fig.1b, where «A1»-«A4» are Semikron SKM400GB17E4 IGBT-modules, «C» – DC-link capacitors assembly of 4 ElectronicON capacitors E50.S34-205NT0 (2 mF), «S» are IGBTs and «D» are freewheeling diodes respectively. Modules «A1» and «A2» are connected in parallel as «A3» and «A4» so transistors «S_j» and «S_j'» operates simultaneously (j=1,2,3,4). Post-fault mechanical bypass is denoted by «QS».

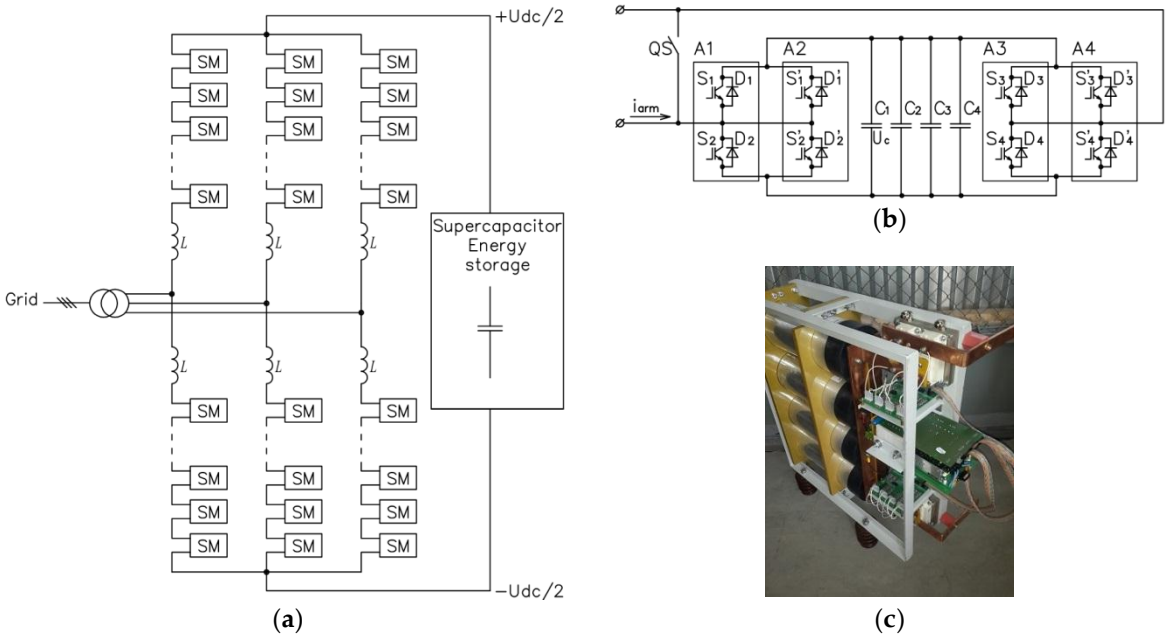

Figure 1. (a) converter scheme; (b) submodule scheme; (c) submodule design

III. ELECTRICAL MODES OF DEVELOPED CONVERTER

Electrical modes of converter SM are defined by arm current, PWM and DC-link voltage of SM. Assuming negligible voltage drop on the arm reactor compared to rated AC voltage the following expression is valid:

$$U_{\Sigma} \approx U_{mac} \cdot \sin(\theta(t)) + U_{dc}/2, \quad (1)$$

where U_{Σ} – sum of all instant SM voltages in arm; U_{mac} – magnitude of phase AC voltage; U_{dc} – instant DC voltage of energy storage; $\theta(t)$ – instant phase of grid AC voltage. Arm current i_{arm} contains both DC an AC component in general case:

$$i_{arm} = I_{mac} \cdot sin(\theta(t) + \varphi) + I_{dc}, \quad (2)$$

where I_{mac} – AC component magnitude; I_{dc} – DC component of arm current; φ – current/voltage phase shift.

In this paper a number of assumptions used. First, only quasi-static modes of converter operation are considered when active power averaged on a fundamental frequency is equal to power losses negligible to apparent power produced by submodule. Also it is assumed that circulating currents are regulated by control system and these currents are utilized for vertical and horizontal energy balancing [7]. And at last we assume that mode is balanced so circulating currents equal zero. Under these assumptions energy balance equation is as follows:

$$I_{mac} \cdot U_{mac} \cdot cos(\varphi)/2 + I_{dc} \cdot U_{dc}/2 = 0 \quad (3)$$

Provided that the alternating current of the phase of the converter is divided equally between upper and lower arms after substituting (3) into (2) for parameters given in Table 1, the following equation may be obtained:

$$i_{arm}(t) = 290 \cdot [\sin(\theta(t) + \varphi) + 0{,}51 \cdot \cos(\varphi)], \quad (4)$$

where $cos(\varphi)$=0 if power conditioner operates as active filter and $cos(\varphi)$=0.5 while is operates as UPS.

IV. PWM ALGORYTHM

Phase shifted PWM is exploited in this work so arm reference voltage splits equally between all N arm submodules. Equation (1) under parameters given in Table 1 results in:

$$V_{ref} = U_{\Sigma}/N = 590 \cdot sin(\theta(t)) + 480. \quad (5)$$

PWM block scheme is shown in Fig.2, where Vcap – measured DC-link capacitor voltage of SM, Vcapref – set point of SM DC-link voltage, Iarm – measured arm current, Vref – reference SM output voltage, carrsig – 1 kHz carrier signal, BM_Kp – gain of DL-link voltage regulation loop.

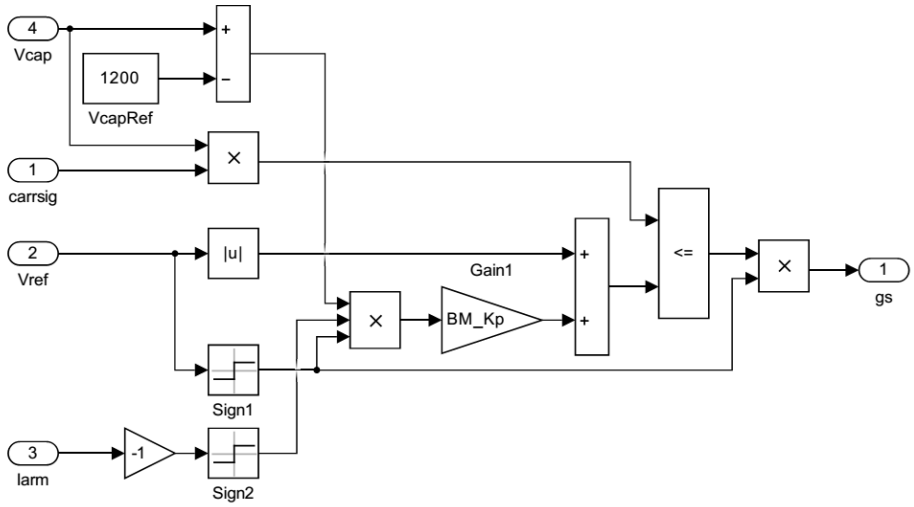

Figure 2. Modulation block

Output signal «gs» may take one of three values: -1, 0, 1 that defines voltage produced by submodule as gs· Vcap. Three of these states can be formed in four ways shown in Table 2. It should be noted that the Table does not include states corresponding to diode mode of operation of the bridge and any abnormal states. Zero state can be formed in two ways – when upper IGBT in each leg of the bridge are switched on (ZT=0) or when lower ones are switched on (ZT=1). This redundancy can be exploited for controlled power loss distribution among different IGBT-modules of the bridge.

Table 2. Submodule IGBT states under normal operation

gs	S_1 & S_1'	S_2 & S_2'	S_3 & S_3'	S_4 & S_4'	Zero type (ZT)
-1	OFF	ON	ON	OFF	-
0	ON	OFF	ON	OFF	0
0	OFF	ON	OFF	ON	1
1	ON	OFF	OFF	ON	-

Five heuristic algorithms of ZT control are compared by power losses and pn-junction temperatures of semiconductor devices. Modes 1 and 2 in Table 3 exploits only one type of zero state when either ZT is constantly zero or ZR is constantly one accordingly. Both types of zero are used for half of period of fundamental frequency in mode 3 while in mode 4 zero type is changed once in two cycles. Fast zero type shuffling is used in mode 5 resulting is more averaged but higher losses.

Table 3. ZT Modulation

PWM mode	ZT definition
1	$\mathrm{ZT(t)} = 0$
2	$\mathrm{ZT(t)} = 1$
3	$\mathrm{ZT(t)} = 0.5 \cdot (1 + \mathrm{sign}(\mathrm{dI_{arm}}/\mathrm{dt}))$
4	$\mathrm{ZT(t)} = 0.5 \cdot (1 + \mathrm{sign}(\sin(50 \cdot \pi \cdot \mathrm{t})))$
5	$\mathrm{ZT(t)} = 0.5 \cdot (1 + \mathrm{sign}(\sin(1000 \cdot \pi \cdot \mathrm{t})))$

V. ELECTRICAL AND THERMAL MODELS

Electrical test model was developed by means of Matlab, where the scheme shown in Fig.2 was assembled of standard SimPowerSystems blocks. Submodule current is provided by controlled current source connected in series with tested submodule while current reference is given by (4). PWM block shown in Fig.3 is implemented in Simulink where the voltage reference is given by (5).

Both power losses and semiconductor pn-junction temperatures of semiconductor devices are calculated by means of Simulink environment. It is assumed in the calculations that the losses in power semiconductor devices include switching and conducting state losses. Conducting losses P_c are expressed as follows:

$$P_\mathrm{c}(t) = \left(\mathrm{V_0} + \mathrm{r} \cdot \mathrm{i(t)}\right) \cdot i(t), \tag{6}$$

where $\mathrm{V_0}$ – maximum rated threshold voltage and r – maximum rated slope resistance valid for 150 ^{0}C. Switching losses P_sw are defined as follows:

$$\mathrm{P_{sw}(t)} = \mathrm{E_{sw}\,(i)}/\tau \cdot \delta(\mathrm{t}). \tag{7}$$

where E_{sw} (i) – turn-on and turn-off power dissipation of IGBT and reverse recovery energy of free willing diode dependencies on current according to datasheet, τ – simulation step size, $\delta(t)$ is equals 1 if commutation occurs at instant t, 0 – elsewhere. Linear approximation of power dissipation on current is used. Backward Euler method with fixed step size of 1 us is used for transient processes calculation. Semiconductor switching instant is detected when current rate of rise exceeds predefined rate of 1 A/us.

PN-junction to case temperature differential is calculated as output of transient thermal impedance transfer function while total power losses are fed into input. Transient thermal impedance transfer function in Foster equivalent network form [8] is expressed as follows:

$$Z(t) = \sum R_i \cdot (1 - \exp(-t/T_i)), \quad (8)$$

where transistor and diode transient thermal impedance parameters and power losses model parameters are given in Tables 4-6.

TABLE 4. Transistor transient thermal impedance parameters

№	Parameter	Value	Unit
1	R(IGBT)1	0.05774	K/W
2	R(IGBT)2	0.00530	K/W
3	R(IGBT)3	0.00134	K/W
4	R(IGBT)4	0.00010	K/W
5	T(IGBT)1	0.02876	S
6	T(IGBT)2	0.00086	S
7	T(IGBT)3	0.00154	S
8	T(IGBT)4	0.00048	S

TABLE 5. Diode transient thermal impedance parameters

№	Parameter	Value	Unit
1	R(FWD)1	0.10800	K/W
2	R(FWD)2	0.01938	K/W
3	T(FWD)1	0.03354	S
4	T(FWD)2	0.00139	S

TABLE 6. Power loss model parameters

№	Parameter	Value	Unit	Notes
1	Eon	156.5	mJ	Ic=400A, Vcc=1200, Tj=150 deg
2	Eoff	180	mJ	
3	Err	130	mJ	
4	V_{ce0}	0,9	V	
5	r_{ce}	4.5	mOhm	
6	V_{f0}	1,22	V	
7	r_f	3.4	mOhm	

VI. COMPUTER MODELING RESULTS

Calculated results for five PWM types under consideration are given in Table 7 witch shows that the least power losses equal to 560 W are obtained for constant zero type algorithms 1 and 2 while zero type algorithm №3 yields the least peak temperature difference equal to 22.1 K. PWM mode №5 gives the highest power losses of 663 W that is 18% higher than modes 1 and 2 with the least power losses. PWM mode №4 combines benefits of other zero type control strategies, namely IGBT-module losses are only 4 W higher compared to strategies with the lowest power losses so the difference is less then 1%, but at the same time the proposed strategy gives only 1.6 K higher temperature difference compared to the strategy №3.

TABLE 7. PWM modes comparison

PWM type		1		2		3		4		5	
cos φ		0	0,5	0	0,5	0	0,5	0	0,5	0	0,5
dT(j-c), K	TV1.1	10,6	18,4	6,6	7,1	8,0	9,1	14,3	11,2	16,6	14,3
	DV1.1	23,3	12,5	13,0	9,2	16,8	20,9	11,2	20,9	12,4	11,2
	TV1.2	0,2	0,0	9,0	4,0	6,1	5,8	2,5	6,7	3,2	2,5
	DV1.2	1,3	4,2	17,2	32,3	13,0	12,7	22,4	12,7	22,4	22,4
	TV4.1	9,0	4,0	0,2	0,0	4,4	5,7	2,5	6,8	3,2	2,5
	DV4.1	17,2	32,3	1,3	4,2	10,0	12,6	23,7	12,9	23,1	23,7
	TV4.2	6,6	7,1	10,6	18,4	10,7	9,0	14,2	11,0	16,0	14,2
	DV4.2	13,0	9,2	23,3	12,5	22,1	20,6	11,1	21,3	12,4	11,1
Pav,W	HB1	248	288	312	331	280	297	286	310	330	363
	HB2	312	331	248	288	298	339	282	313	333	364
	∑	560	619	560	619	578	635	568	623	663	727

The dependency of the hottest pn-junction temperature difference on time for PWM types 3 and 5 under cos(φ)=0.5 is shown in Fig.3, witch clearly evidence that temperature variation period is defined by ZT variation period in this cases.

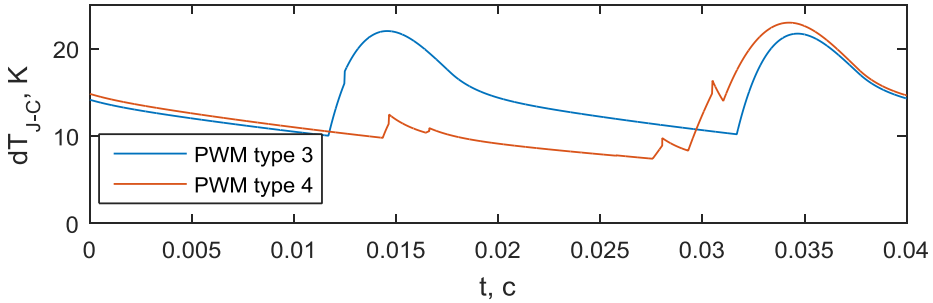

Figure 3. Temperature different dependency on time for main PMW types

VII. CONCLUSION

The proposed modification of PWM zero state redundancy algorithm gives 8.6 ^{0}C reduction of the highest pn-junction temperature compared to PWM strategy without losses balancing while total losses of submodule increase less then 1%. This method utilizes variation of zero type changing one in two cycles. Obtained results are valid for the particular full-bridge MMC submodule. Calculations should be performed is the same way as described if other PWM switching frequency or other IGBT-module parameters are exploited.

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