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A Noble Design of First Order Sigma Delta Modulator

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Abstract

This paper reports a noble design of first order sigma delta modulator using 0.5 micron technology. We have mainly concentrated for high resolution Sigma Delta Analog to Digital Converters. In this design we have considered the low power consumption & high signal to noise ratio (SNR). Simulation results are presented by 0.5 micron technology, using two stage CMOS op-amp in integrator stage with gain of 70 db. By considering ± 2.5 supply voltage, 256 oversampling ratio we achieved 10 bit resolution & low power consumption of 6.8 mW. Design has been carried out in Tanner tool using HP 0.5 micron technology. Simulation results are verified using S-Edit and W-Edit.

Keywords: Sigma delta modulator, SNR, Low power consumption, S-Edit, W-Edit.

Introduction

Analog to digital converters (ADC) is an important device widely used in many electronics & instrumentation systems for interfacing between analog electronics with digital electronics. In practical applications an ADC is exposed to time varying signal instead of DC signals. Sigma delta modulation technique is widely employed in designing of Sigma Delta ADCs (SDADCs) in several years, it is very suitable for converting low bandwidth signal such as audio frequency & biomedical signal in digital form. SDADCs have more advantages than the other ADCs. It has required less analog component & most of the design is in digital part so the designing of SDADCs is simple & it has high resolution. Power consumption & signal to noise ratio (SNR) is crucial factor for high performance & error free design. SDADCs consists of a Sigma Delta modulator followed by a decimation filter. The Sigma Delta modulator samples the input signal at many times the Nyquist rate a process referred

to as oversampling and performs very coarse analog to digital (A/D) conversion on the resulting narrow band sequence. Through the use of coarse digital to analog (D/A) conversion and feedback, the quantization error introduced by the coarse A/D converter is spectrally shaped a process referred to as quantization noise shaping. The decimation filter removes the out-of-band portion of the quantization error and reduces the output rate to the Nyquist rate of the input signal [1]. The block diagram of SDADCs is shown in Fig. 1.

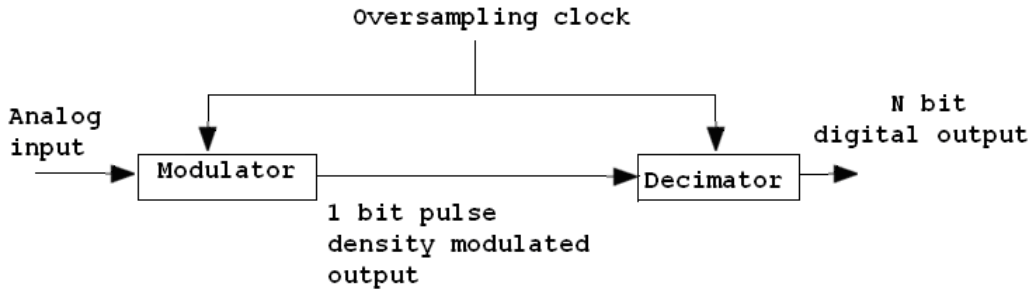

Figure 1: Block diagram of a SDADCs.

First Order Sigma Delta Modulator

Sigma delta modulator is the analog part of SDADCS. A block diagram of a basic first order sigma-delta modulator is shown in Fig. 2 [2]. It consists of an integrator and a 1-bit ADC in the forward path and a 1-bit DAC is in the feedback path of a single-feedback loop system. When the integrator output is greater than the reference voltage at the comparator input, the comparator gives an output 'high'. This output high controls the DAC which gives an output of + Vref which is subtracted from the input of the modulator in order to move the integrator output in the negative direction [3], [4], [5]. Similarly when the integrator output is less than the reference voltage at the comparator input, the feedback path moves the integrator output in the positive direction. The integrator therefore accumulates the difference between the input and quantized output signals and tries to maintain the integrator output around zero.

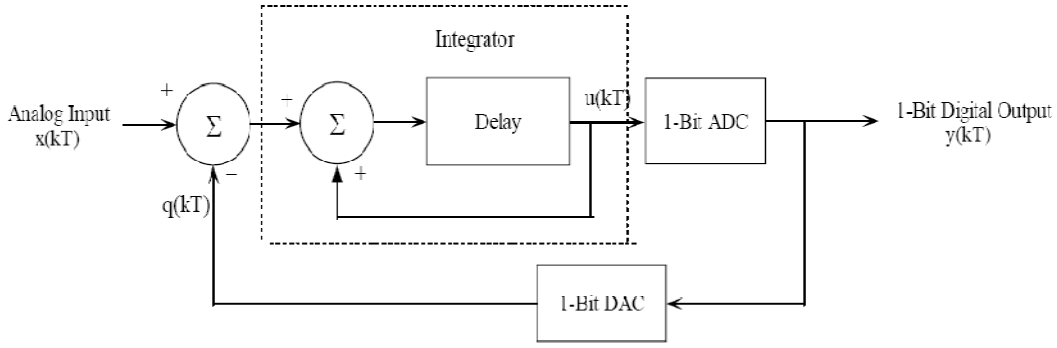

Figure 2: Block diagram of a First Order Sigma Delta Modulator.

$$y(kT) = x(kT - T) + Q_e(kT) - Q_e(kT - T) \tag{1}$$

Where k is an integer constant,
T is the inverse of the sampling frequency,
y(kT) is the output of the modulator at instant kT,
x(kT-T) is the input of the modulator at instant kT-T,
$Q_e(kT)$, $Q_e(kT-T)$ are the quantization errors of the ADC at instant kT and kT-T

Equation.1 can be written in Z domain is:

$$Y[z] = z^{-1}X[z] + (1 - z^{-1})Q_e[z] \tag{2}$$

Where Y(z), X(z) and $Q_e(z)$ are the z-transforms of the modulator output, input and quantization error respectively. z^{-1} is called the Signal Transfer Function (STF) and represents a unit delay. The term $(1 - z^{-1})$ is called the Noise Transfer Function (NTF) and has a high-pass characteristic, allowing noise suppression at low frequencies [6].

Proposed First Order Sigma-Delta Modulator Design

The delta sigma modulator is the core of delta sigma converters. As mentioned above it produces a bit stream corresponding to input signal applied. The average level of this bit stream represents the input signal level. Proposed design of first order delta sigma modulator is shown in Fig. 3. The design of modulator consists of one integrator, comparator, d flip-flop and 1-Bit DAC to achieve required function. For the designing of this component we used the 0.5 micron CMOS technology. And simulation is performed by using Tanner tool with TSPICE simulator. Simulation of first order sigma delta modulator is done by applying Sine wave of 1 V peak-to-peak voltage to the input of the modulator, simulated results of modulator is shown in the section 4.

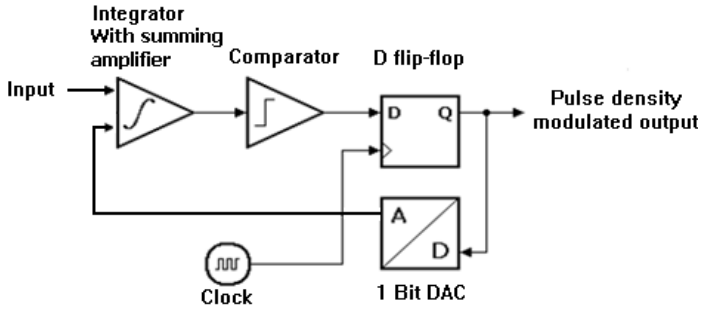

Figure 3: Block representation of proposed first order analog delta sigma modulator
In this section, a Continuous Sigma Delta Modulator has been implemented. The circuit design of various components has been discussed in the subsequent sections.

Integrator design

Integrator is the main building block in the modulator design in which output voltage is directly proportional to the integral of the input and it acts as a low pass filter. Integrator design consists of one CMOS op-amp in the inverting mode with the feedback resistor R_F replaced by a capacitor C_F, the gain of the loop should be one. This architecture contains combined first order loop so the noise of the first stage cancel out, and the loop has second order noise shaped error. To achieve a gain of one, the integrator gain factor T/RC is formed from time domain analysis, and set to one. For a given clock period, R and C values can be calculated. In a practical integrator, to reduce the error voltage at the output, a resistor R_F is connected across s the feedback capacitor C_F. Thus R_F limits the low frequency gain and hence minimizes the variations in output voltage. Considering frequency response the limiting frequencies are defined as follows. The frequency at which gain is 0 dB is given by-

$$f_b = \frac{1}{2\pi R_1 C_F}$$

Where R_1 is input resistor and C_F is feedback resistor.

The gain limiting frequency is given by-

$$f_a = \frac{1}{2\pi R_F C_F}$$

The value of f_a and in turn $R_1 C_F$ and $R_F C_F$ values should be selected such that

$$f_a < f_b .$$

This integrator also works as a summing amplifier which is summed up the input signal and the output of 1 bit DAC used in the design.

For designing of CMOS op-amp two stage CMOS op-amp design technique is used. Two stage CMOS op-amp have sufficient gain to effectively carry out integration operation as well as enough bandwidth to support input signal. Circuit level design of two stage CMOS op-amp is shown in Fig. 4 CMOS op-amp have gain of 70 dB. Frequency response of op-amp and slew rate results is shown in the Fig. 5. W/L ratio of all the transistors used in the op-amp design is calculated by two stage CMOS op-amp design technique to perform required function as well as power consumption is also minimize of only 0.685 mW for the power supply range of +/- 2.5 V.

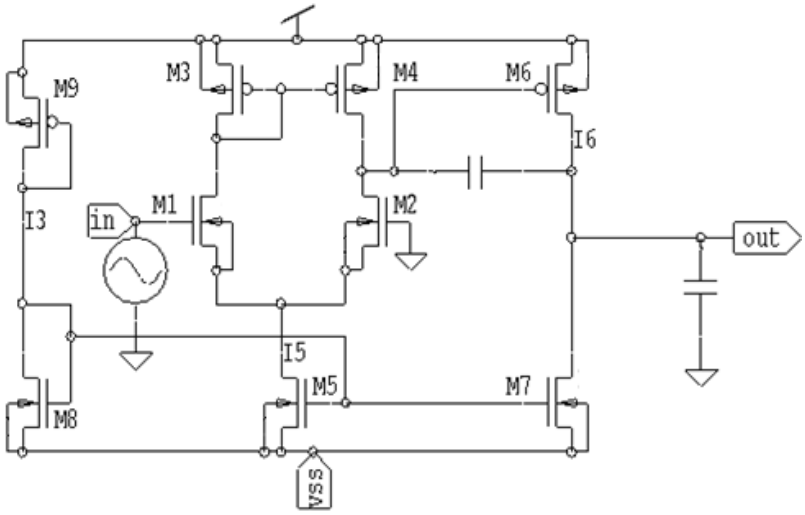

Figure 4: Design of two stage CMOS Op-amp.

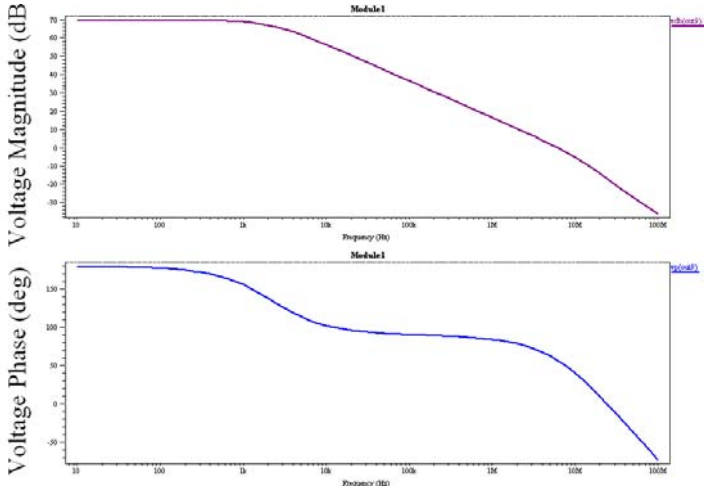

Figure 5: AC response of two stage CMOS Op-amp.

Comparator design

A comparator acts as the quantizer in the first order modulator. Since the comparator is of 1-bit it has only two levels either a '1' or a '0'. A '1' implies that V_{DD} = + 2.5V and a '0' implies that V_{SS} = - 2.5V. If the output of the integrator is greater than the reference voltage (V_{ref}) is has to give an output of '1' and if the integrator output is less than reference voltage then the output of the comparator should be '0'. A simple comparator performs the required function efficiently. Given a reference level, a comparator gives an output of V_{DD} when the signal is greater than the reference level and an output of V_{SS} when signal is less than reference level. In this design the V_{ref} = 0V. The operational amplifier can be used as a comparator. The only change needed is that the comparator doesn't require the compensation capacitor which is required by

the operational amplifier. The comparator circuit is shown in Fig. 6. The comparator in the modulator will be driving the 1-bit DAC and also any buffer present at the output of the modulator. Here we give the sine wave input of 5 kHz frequency in the IN2 terminal of the comparator & obtained the output as shown in Fig. 7.

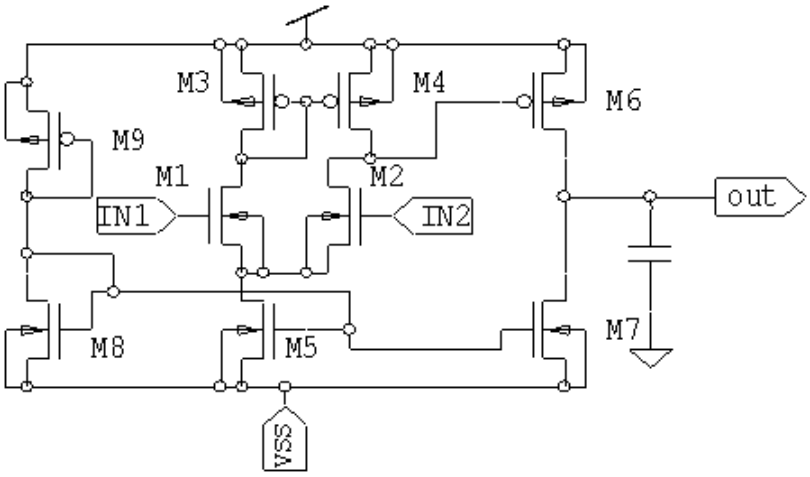

Figure 6: Design of 1-Bit Analog to Digital Converter (Comparator).

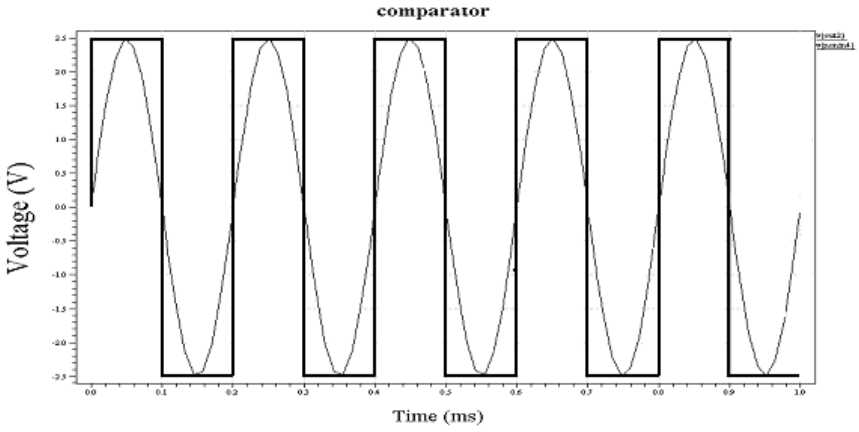

Figure 7: Comparator output for the sine wave of 5 KHz frequency.

D Flip-Flop design

The circuit level design D flip-flop used in the first order modulator design is as shown in Fig. 8. D flip-flop is acts as a sampler which latched the input for one clock period. Here we apply the output of comparator to the d input of the circuit, and takes the output from q & qbar. It is generally an edge-triggered flip-flop which gives output for the positive transition of the clock and operated with oversampling clock. The output of D flip-flop is as shown in Fig. 9.

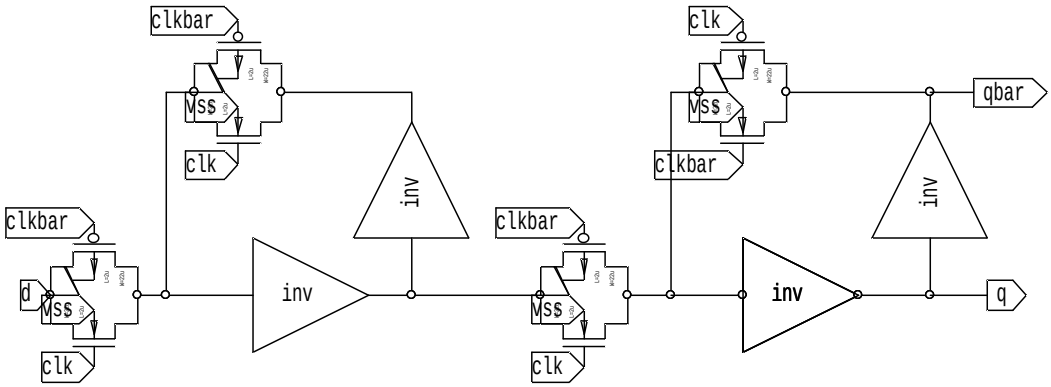

Figure 8: Design of D flip-flop.

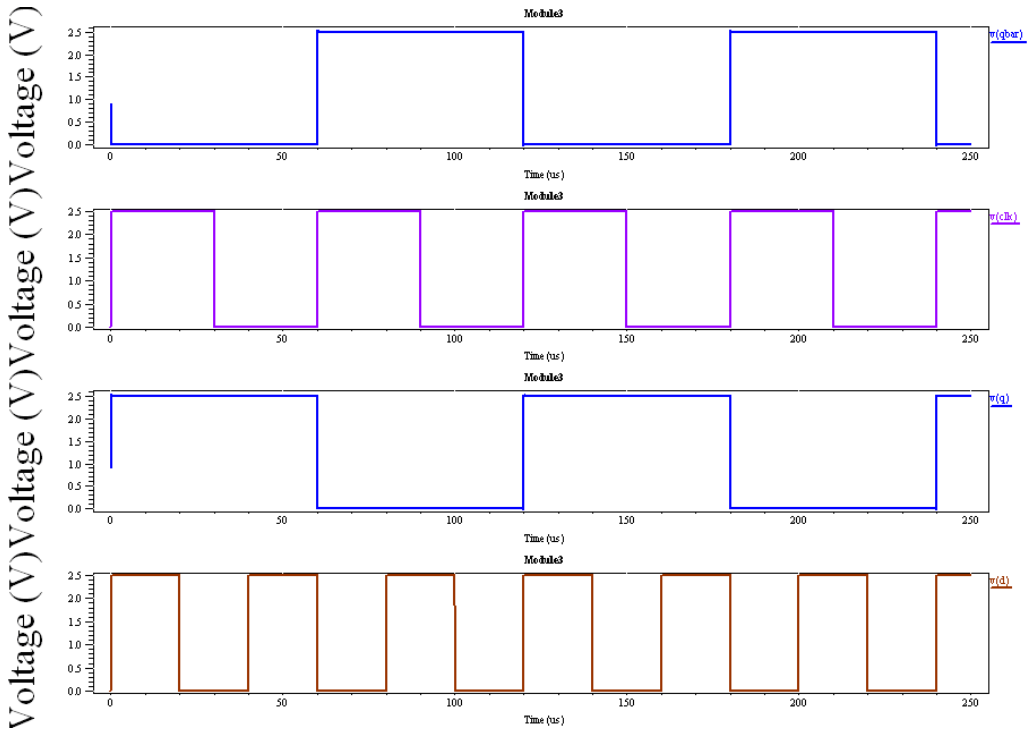

Figure 9: Result of D Flip Flop.

1-Bit Digital to Analog Converter (DAC) design

The digital to analog converter is necessary to convert the - 2.5 to + 2.5 V signal at the output to a - 0.35 to + 0.35 V signal to be subtracted from the input. The DAC must reference the feedback signal in the modulator so that the difference at the integrating amplifier does not saturate the amplifier. The DAC consists of two transmission gates and two pairs of resistors as shown in Fig. 10. Simulated result of DAC is as shown in Fig. 11. The gate of the NMOS transmission gate 1 is tied to the gate of the PMOS on transmission gate 2. Likewise, the gate of the PMOS on transmission gate 1 is tied to

the gate of the NMOS on transmission gate 2. The first pair of gate is driven by q from the output of D flip-flop. The second pair of gates is driven by qbar from the output of the D flip-flop. qbar is the inverse of q, so this design turns only one transmission gate ON at a time. The input to each transmission gate is a voltage divided down from the positive and negative 2.5 V rails. This voltage division is accomplished using a 0.14 KΩ resistor tied to ground and a 0.86 KΩ resistor connected to the respective rail.

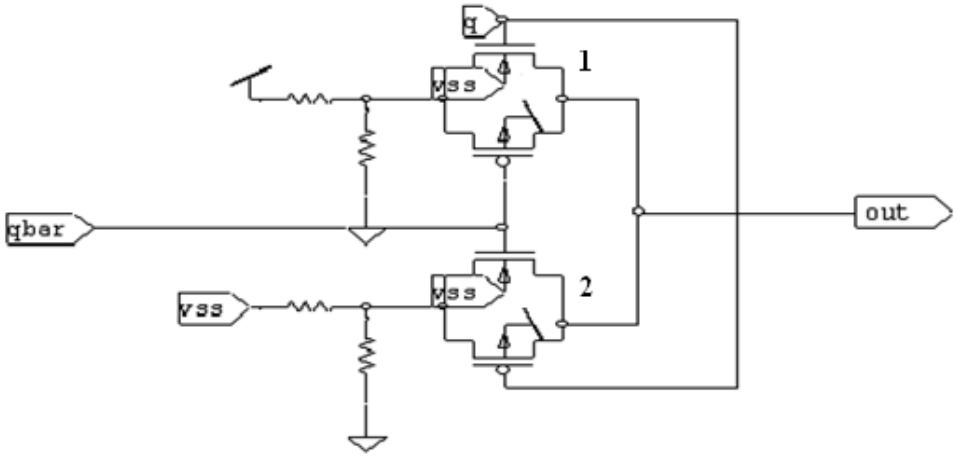

Figure 10: Design of 1-bit digital to analog converter.

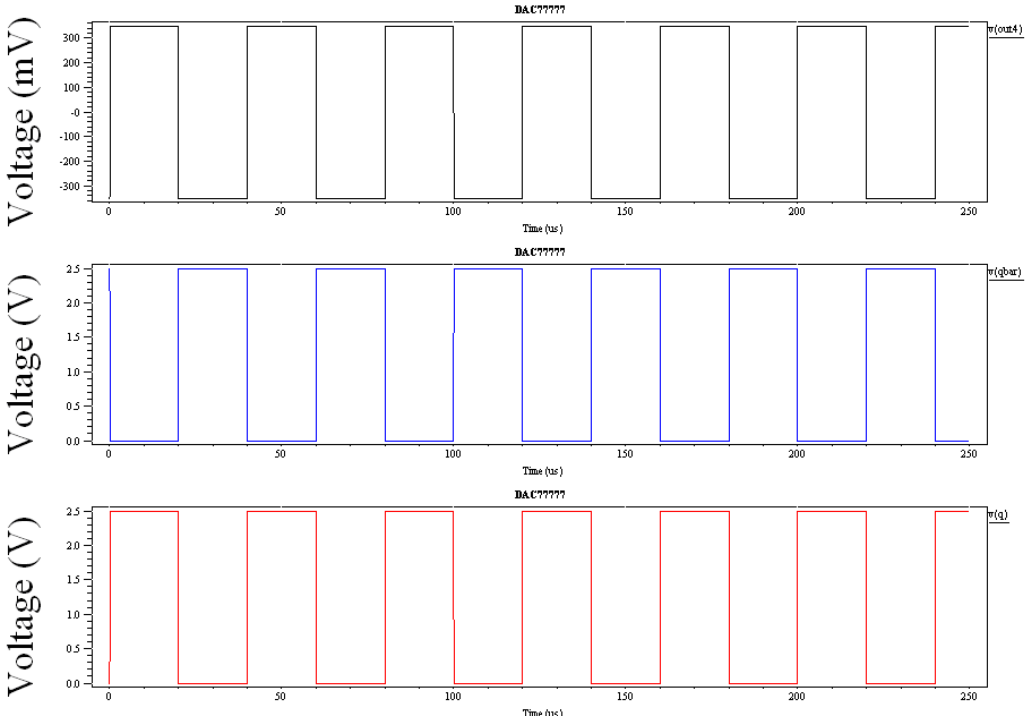

Figure 11: Results of 1-bit digital to analog converter.

Simulation results

Simulated results for the first order sigma delta modulator are determined. Here we apply the sine wave of 10 KHz frequency with amplitude of 1V peak to peak to the input of the modulator. Sine wave completes its one cycle in the period of 100 µs and corresponding output waveform for this period is as shown in Fig. 13. The clock input gives to D flip-flop of oversampling frequency 5.12 MHz for the oversampling ratio of 256. The first order modulator operated with the power supply range of + 2.5 V (Vdd) to – 2.5 V (Vss). The output of the modulator is pulse density modulated signal. As the input increases the positive pulse width increases and at the peak of the sine wave the positive pulse width has the maximum width. As the input decreases the positive pulse width decreases and when the input reaches zero the positive pulse width becomes equal to the negative pulse width. As the sine wave decreases below zero the negative pulse width of the output increases and reaches a maximum when the sine wave reaches the negative peak. The average value of the output follows the analog input. Average power consumption of the modulator is determined from the Netlist output file of the TSPICE simulator for the period of input one cycle is 6.8 mW.

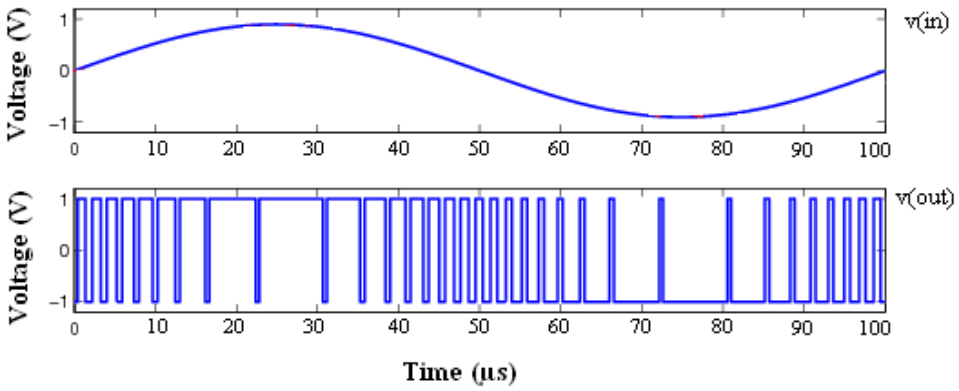

Figure 12: Results of first order sigma delta modulator.

Conclusions

First order Sigma Delta Modulator has been successfully designed & simulated by using 0.5 micron technology with the help of Tanner tool & TSPICE simulator. Simulated results are verified using S-Edit for schematic design & W-Edit for waveform analysis. For design of complete sigma delta modulator we have designed the one two stage CMOS op-amp with DC gain of 70 dB & power consumption of 0.685 mW. 1-Bit DAC using transmission gate & resistor and one positive edge triggered D Flip-flop. By using power supply of ± 2.5 V for complete modulator design with oversampling ratio of 256 & oversampling frequency of 5.12 MHz we have achieved resolution of 10 Bit, SNR of 86.04 db and low power consumption of 6.8 mW.

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