International Journal of Electrical Engineering.
ISSN 0974-2158 Volume 10, Number 3 (2017), pp. 323-335

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Minimizing the Sub Threshold Leakage for High Performance CMOS Circuits Using Stacked Sleep Technique

Kalasapati Bindu Madhavi*

Mamidala Pallavi*

Velicharla Moshe Rani*

Abstract

In CMOS circuits, the reduction of the threshold voltage due to voltage scaling leads to increase in sub threshold leakage current and hence, static power dissipation. For the most recent CMOS feature sizes (e.g., 45nm and 65nm), leakage power dissipation has become an overriding concern for VLSI circuit designers. ITRS reports that leakage power dissipation may come to dominate total power consumption [1]. In the nanometer technology regime, power dissipation and process parameter variations have emerged as major design considerations. These problems continue to grow with leakage power becoming a dominant form of power consumption. Leakage power dissipation is projected to grow exponentially in the next decade according to the International Technology Roadmap for Semiconductors (ITRS).This directly affects portable battery operated devices such as cellular phones and PDAs since they have long idle times. Several techniques at circuit level and process level are used to efficiently minimize leakage current which lead to minimize

the power loss and prolong the battery life in idle mode. This paper presents a technique for minimizing sub threshold leakage current using stacked sleep technique. Comparison is made with conventional CMOS, Sleepy stack, Forced stack, Sleepy keeper and the proposed body biased keeper which were analyzed using BSIM 4 model. The proposed technique dissipates lesser static power and lesser delay product compared to the previous technique. An improvement of 1.2X was observed in static power dissipation in comparison with conventional approach, thus maintaining the state of art of the logic in the digital circuit.

Keywords: Low Power, Gate oxide Tunneling, sleep mode, idle mode, Sub threshold leakage, Conventional CMOS, Sleepy stack, Forced stack, Body biased keeper, Sleepy keeper, BSIM 4

INTRODUCTION

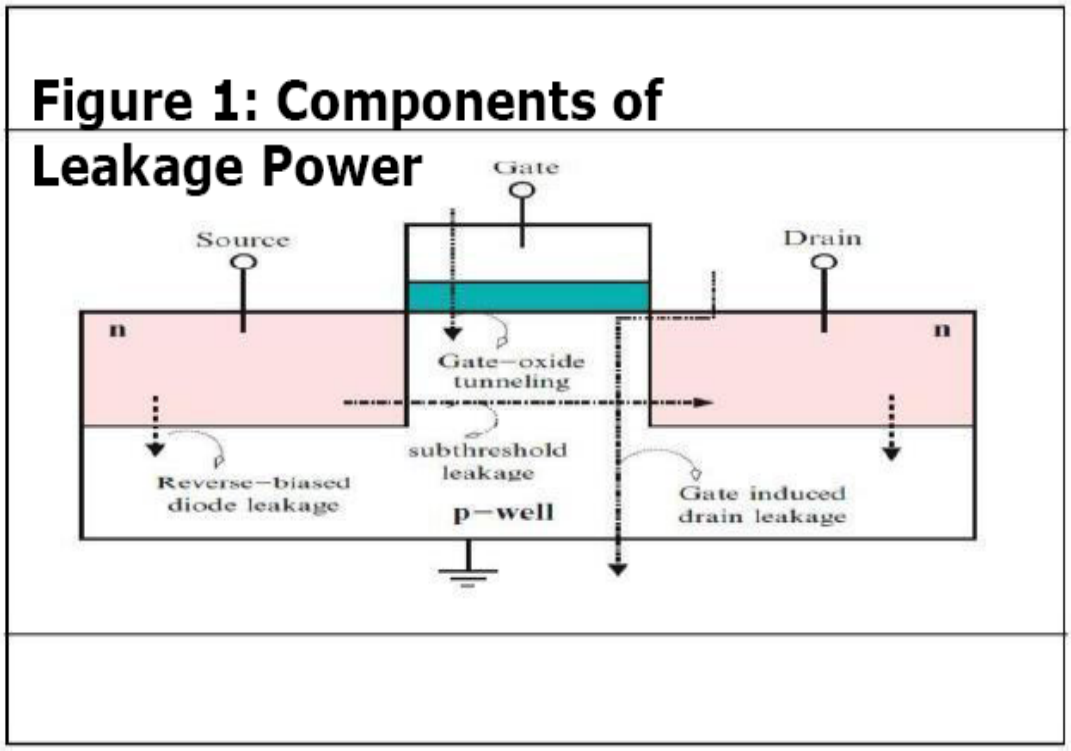
With ever increasing in high speed computation and battery operated devices like laptops, tablet, palmtops, note books etc., power consumption has become major concern in very large scale integration (VLSI) systems. Also power consumption is major concern in deep sub micron technologies.

According to Moore's law "number of transistor increases exponentially double every two years" (Borkar, 2001; and Srivastava *et al*., 1998). Thus shrinkage in size and addition of large function in an integrated circuit gives more power dissipation. Power consumption in VLSI circuits includes static (or leakage) and dynamic power dissipation, short circuit power dissipation. Switching power which includes both short circuit and dynamic power is consumed when the charging and discharging of the capacitance takes place. Leakage power is due sub threshold leakage and reverse biased diode.

Thus total power consumed by the circuit is given by,

$$P_{total} = P_{dynamic} + P_{short\text{-}circuit}$$

Thus, the leakage power becomes the key to low power design. Leakage power is dissipated when the transistor is in standby mode or in sleep mode. Even though transistor is in stable state, it produces small leakage current at the junctions and also reverse biased diode is the major contributor of this leakage current (Figure 1).



This paper thus concentrates on reducing the leakage power at the dynamic node by placing the body biased keeper. By this approach 1.2X power dissipation was observed in comparison with previous approaches.

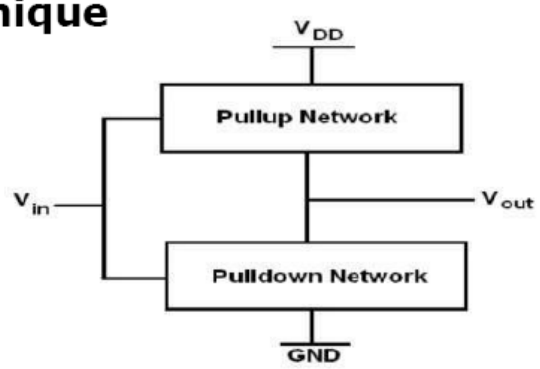
RELATED WORK

In this section the previously applied techniques for sub threshold reduction are briefed.

A. Conventional CMOS Technique (Mutoh S *et al.*, 1995)

Figure 2 shows the block diagram of conventional CMOS logic. In this approach, Pull up network is designed using PMOS transistors and Pull down network is designed using NMOS transistors.

Figure 2: Conventional CMOS Technique

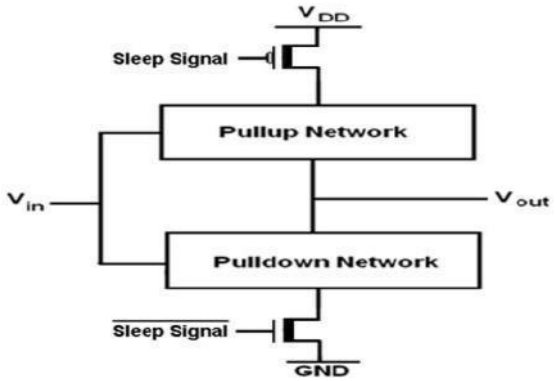


PMOS/NMOS are represented in parallel/series for product and sum term. PMOS is connected to power supply and NMOS is connected to ground.

B. Sleep Transistor technique (Powell *et al*., 2000; and Park *et al*., 2004)

Figure 3 shows the block diagram of sleep transistor technique. A sleep PMOS transistor is placed between power supply V*dd* and the pull up network. Similarly sleep NMOS transistor is placed between ground and pull down network. The sleep transistors function in such a way that they are turned on during the active mode and turned off during the sleep/ in active mode. This technique reduces the sub threshold leakage by isolating the gates from power supply and ground. Hence this technique is also termed as state destructive technique as there is loss in the present state logic.

Figure 3: Sleep Transistor Technique

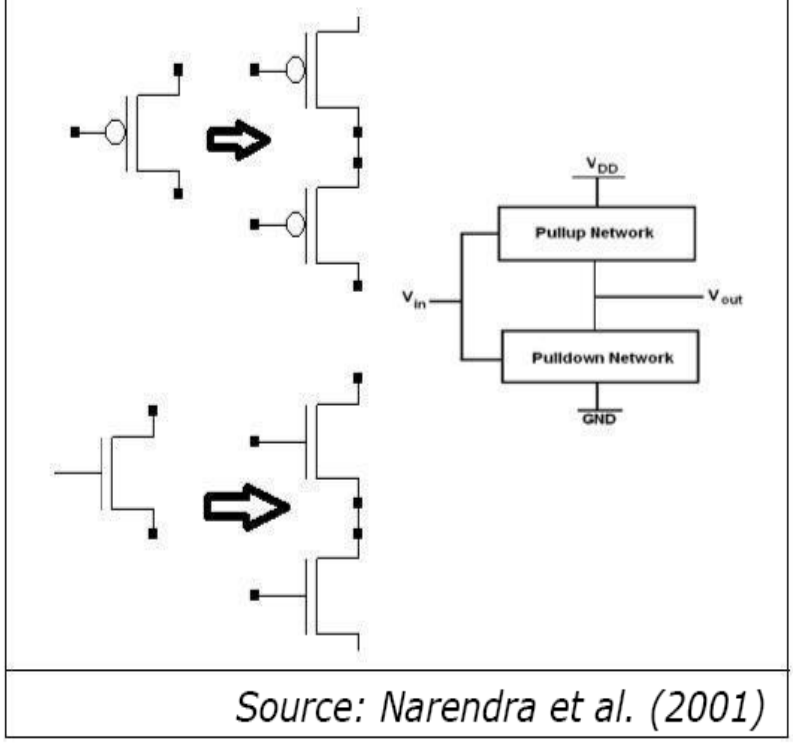


Source: Powell et al. (xxxx) and Park et al. (2004)

C. Forced Stack Technique (Narendra *et al*., 2001)

Figure 4 shows the block diagram of stack approach. In this approach, the circuit is divided and stacked into two half width of the total transistor size. When these are stacked together, the simultaneously turn on and off. Thus reducing the sub threshold leakage current. But the overall delay of the circuit increases as the number of transistor increases.

Figure 4: Forced Stack Technique

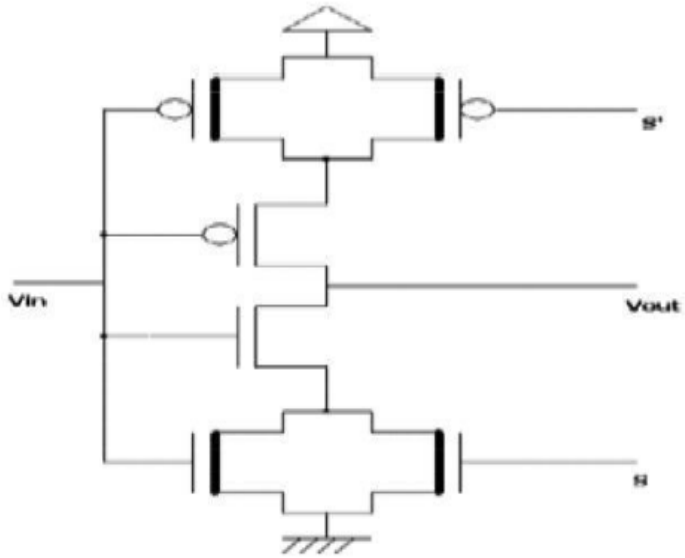


Source: Narendra et al. (2001)

D. Sleepy Stack Technique (Park, 2005; and Kao and Chandra-kasan, 2001)

Figure 5 shows the block diagram of sleepy stack approach. It combines sleep transistor and stack technique. Hence they are called as sleep transistor technique. Here the sleep PMOS is placed parallel to pull up network and sleep NMOS is placed parallel to pull down network. The sleep transistors action are same as in sleep transistor technique. Since sleep transistors are always on in active mode there is current flow in the circuit and hence has faster switching time than stack approach. Here high Vth transistors are used as sleep transistors. As high V^{th} transistors are used leakage is substancially reduced.

Figure 5: Sleepy Stack Technique

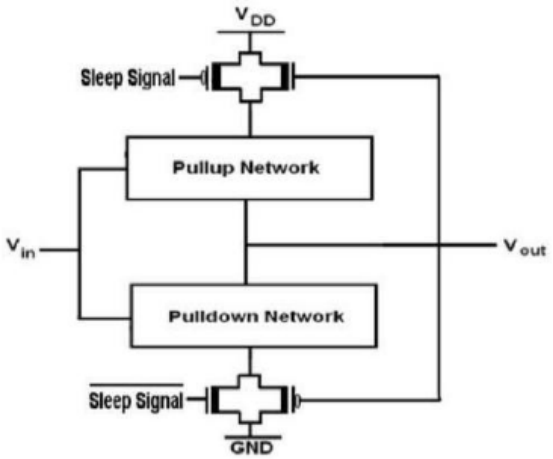


Source: Park (2005) and Kao and Chandrakasan (2001)

E. Sleepy Keeper Technique (Se Hun Kim and Mooney, 2006)

Figure 6 shows the block diagram of sleepy keeper technique. It is the improved version of sleep approach. In this technique, an additional high Vt NMOS transitor is added in parallel with sleep PMOS transistor and high Vt NMOS is added in parallel with sleep PMOS. In sleep mode, sleep transistors are is cut off state. So, when sleep signal is asserted, the high Vt NMOS transistor connected in parallel with the sleep PMOS transistor is the only source of Vdd to the pullup network and the high Vt PMOS transistor connected in parallel with the sleep NMOS transistor provides the path to connect the pulldown network with the ground. Thus the major advantage of this approach is it reduces the leakage power thereby maintaining the logic state of the circuit.

Figure 6: Sleepy Keeper Technique



Source: Se Hun Kim and Mooney (2006)

METHODOLOGY

In this paper, we present stacked sleep transistor technique. In this sleep transistor was getting stacked, which reduces the leakage current to great extent. This technique uses two stacked sleep transistors in power supply rails and two stacked sleep transistor in ground. Thus leakage reduction takes place in two steps. Firstly, due to stack effect of sleep transistor and secondly due to sleep transistor itself. It is well known fact that NMOS are not efficient in passing the power supply. But in this technique, stacked sleep transistor uses pmos in the power supply and NMOS in the ground for maintaining exact logic state of the circuit (Figure 6).

Let us maintain the value of logic 1 in sleep mode. During standby mode, sleep = 0 and sleep bar = 1 is asserted. The stacked sleep approach uses this pmos to get connected to power supply and nmos to be connected the ground. This is the reason why the pmos/nmos is placed in parallel to the sleep transistor. When in sleep mode this pmos is the only source of power supply to pull up network.

Let us now maintain the value of logic 0 in the sleep mode. During this mode, sleep = 1 and sleep bar = 0 is asserted. The stacked sleep trannsistor uses this logic 0 output to maintain the nmos transistor connected to ground ad maintain the logic state equal to logic 0 at the output. Thus when in sleep mode nmos transistor, is the only source of ground to pull down network as the sleep transistor are turned on.

SIMULATION RESULTS

Microwind EDA tool was used for the layout and the simulation of two input NAND gate was done using BSIM 4 MOSFET model in 1.2 nm technology. Performance characteristics such as static power dissipation, dynamic power dissipation, propagation delay and power delay products in static and dynamic conditions were observed using conventional CMOS, Stack, Sleep and Sleepy keeper techniques at a temperature of 27 ^{0}C and a Supply voltage, VDD of 1.2 V.

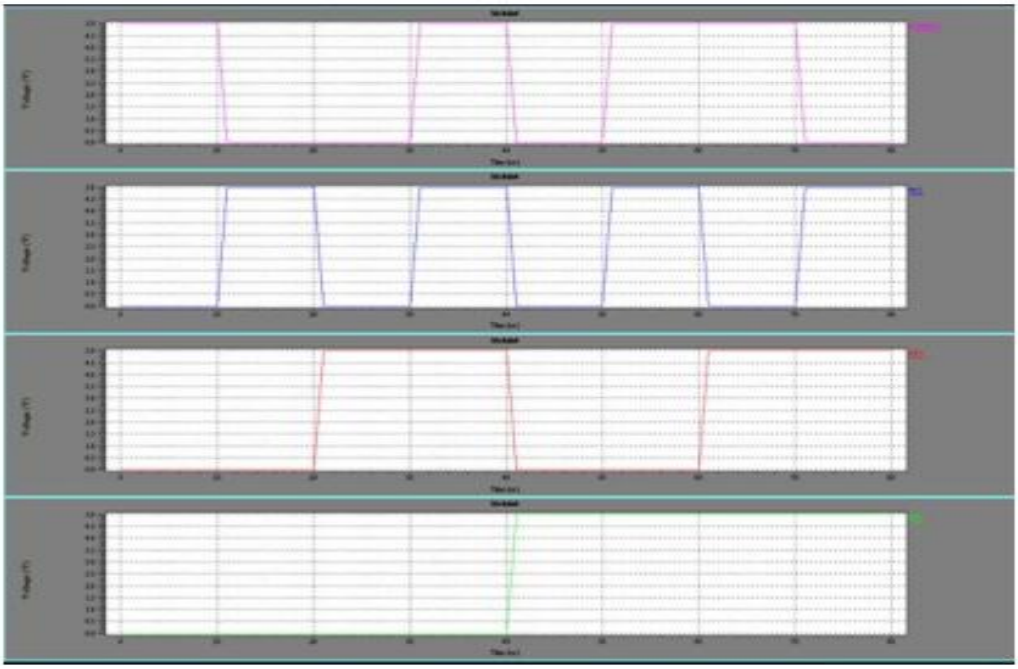
The threshold voltage of MOS transistor increases with increase in its channel length modulation. So the channel length of high threshold transistor and sleep transistor was maintained larger than low threshold transistor in stacked sleep approach. The probable input combinations are shown in table 1.

Table 1: Combination of Input Vector

a	b	Sleep	~Sleep
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

The minimum leakage was found during the initial state when the input vectors are maintained at logic 0. The static power dissipation is calculated as the average of power dissipation for all the input vector combination. The dynamic power dissipation was calculated by applying the clock signals to the input at the temperature of 27^{0}C.

Fig.7. waveform of inverted carry logic using sleepy stack approach



Waveforms for input vector combinations is shown in the Figure 8 and 9. Figure 10 shown the layout of two input nand gate.

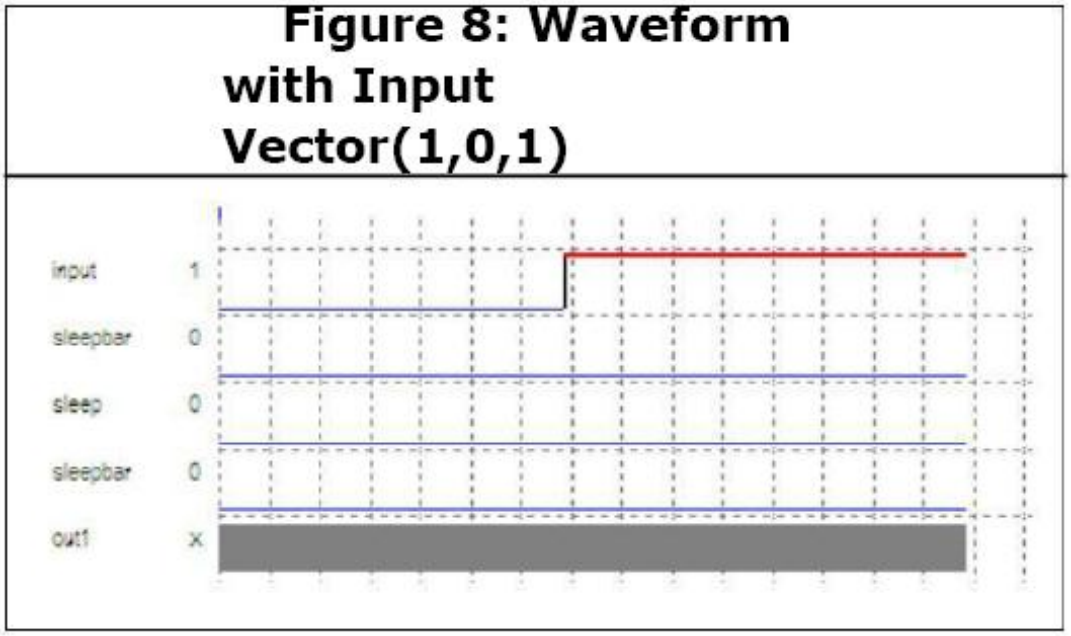


Figure 9: Waveform with Input Vector(1,1,0)

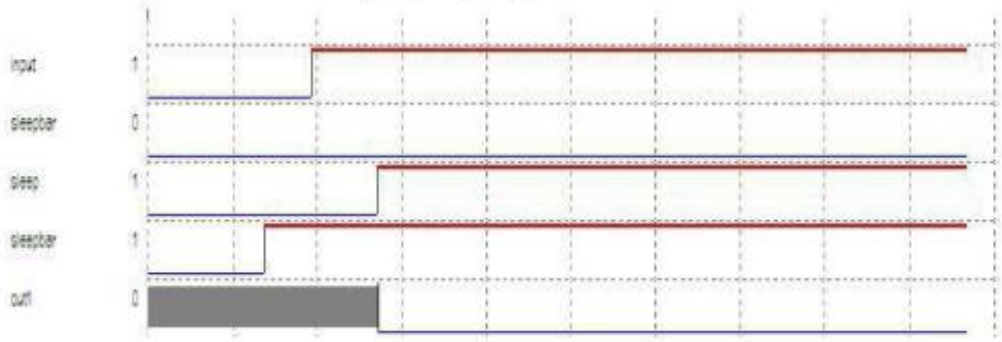
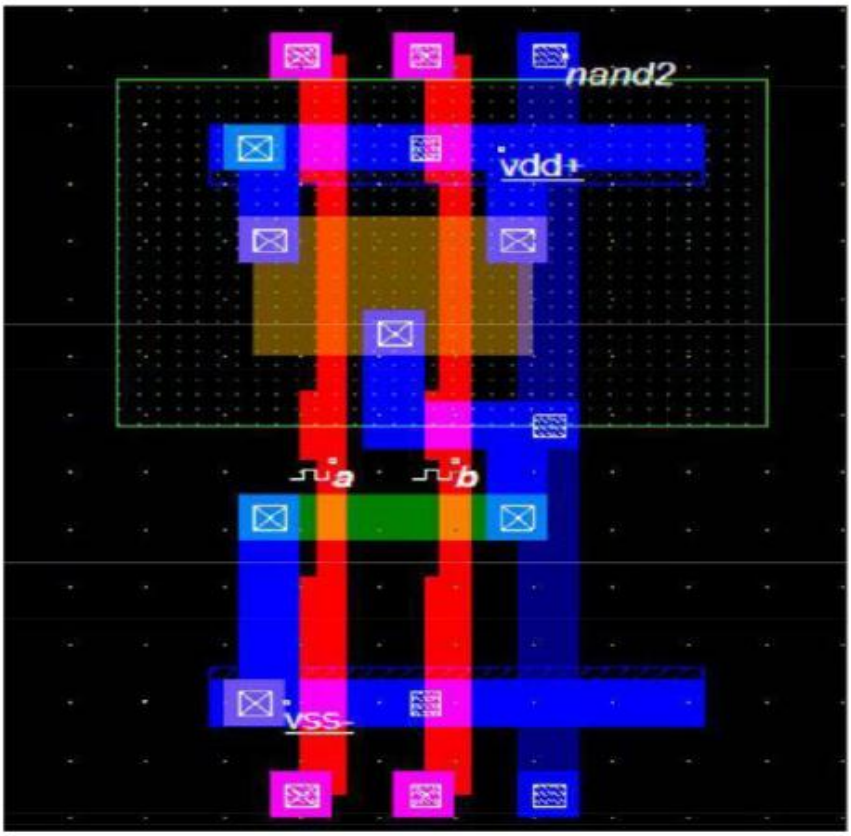


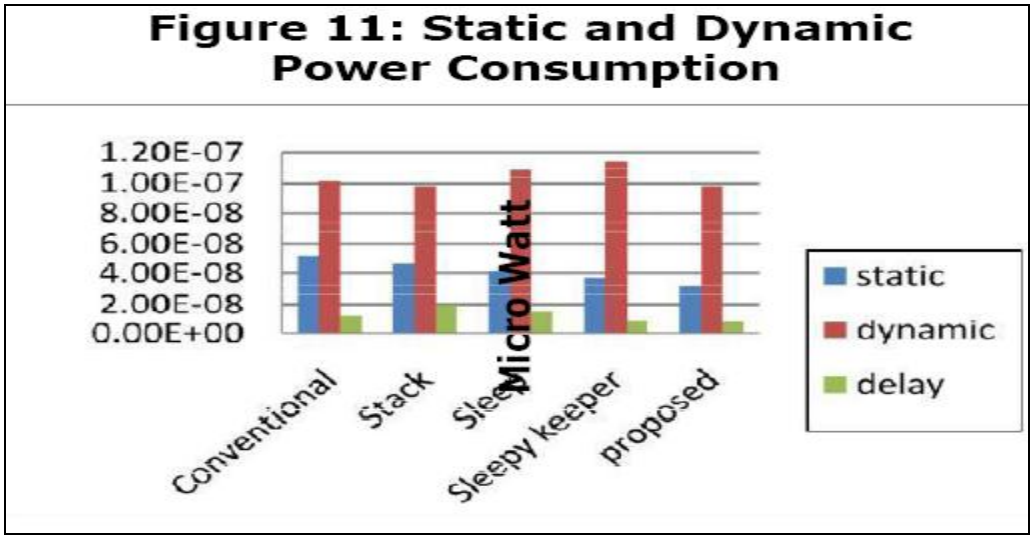
Figure 10: Layout of a Two Input NAND Gate

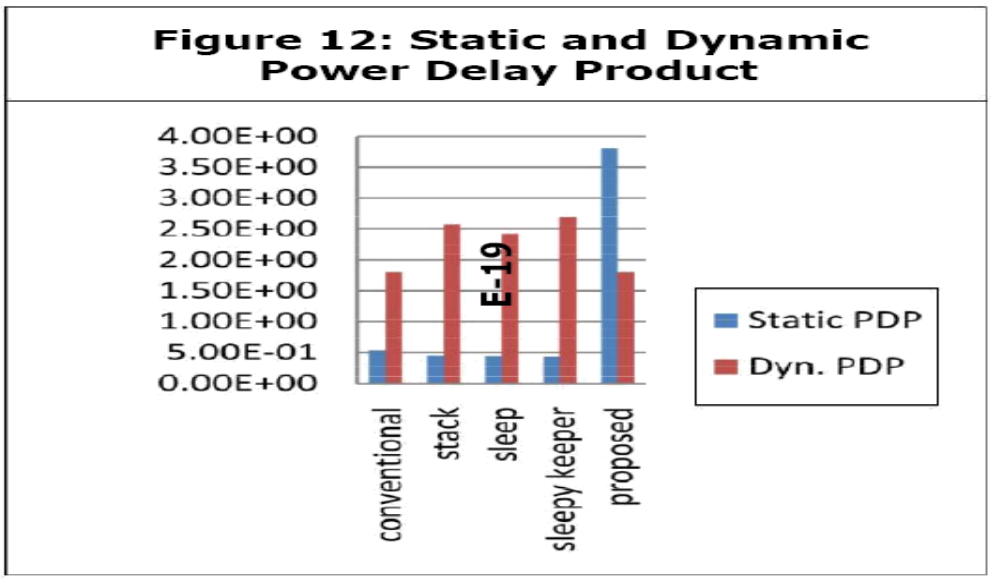


PERFORMANCE COMPARISON

Comparitive analysis is done on NAND2 as the benchmark circuit. Static power dissipation of the NAND2 gate was 0.048 W using the conventional CMOS technique while only 0.032 W static power was dissipated using the Stacked sleep technique. Figures 11 and 12 shows the comparision among different logics for static and dynamic power consumption.

Static power delay product of conventional logic gate and the proposed technique is found to be 0.4304 x 10^{-19} J and 0.42 x 10-^{19} J respectively.





CONCLUSION

Performance characteristics such as static power dissipation, dynamic power dissipation, power, delay, power delay product was analyzed for the conventional CMOS logic, stack, sleeper, sleepy stack, sleepy keeper with the proposed stacked sleep approach in 1.2 nm technology. By experimental result it was found that there was 1.2 X improvement in the power dissipation with the stacked sleeper technique.

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