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A New Three-phase Seven-Level Symmetrical Inverter with Various PWM Control Strategies

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Abstract

This paper deals with three-phase Reverse Voltage Multilevel Inverter with various PWM control strategies. Compared to conventional Diode Clamped, Flying capacitor and cascaded H-bridge multilevel inverters Reverse Voltage MLI requires least number of switches. This paper also presents a comparison of PD, APOD, ISPWM and COPWM techniques for the Reverse Voltage multi level inverter. The effective analysis has been demonstrated by MATLAB/SIMULINK. The THD analysis has been done for different Modulation indices.

Index Terms— Phase Disposition PWM, Alternative Phase Disposition PWM, Carrier Overlapping PWM, Inverted Sine PWM

1 Introduction

In high power applications, multilevel inverters (MLIs) are gaining more importance because of its enhanced harmonic profile and power ratings. The broad classification of multilevel inverters are cascaded H-bridge MLI (CHB), Diode clamped MLI (DC), Flying capacitor MLI (FC) [3]. Among the three MLIs mentioned, CHB MLI is preferred because of its simple structure and no requirement on clamping diodes and capacitors. Cascaded Multilevel inverter, as the name indicates its connection of many single phase inverters in series with other. With respect to voltage source used the CHB MLI can be classified as symmetrical and asymmetrical topology [12]. On comparing both the topologies, asymmetric cascaded MLI is been considered to obtain more number of output voltage levels, which can be obtained with definite number of switches.

Researchers have proposed numerous multicarrier pulse width modulation techniques on multilevel inverter, in order to work at higher voltage and power than regular two level converters. The output voltage of a multilevel inverter is a staircase structure, which resembles sine waveform. In this staircase format, each step refers a level. Increase in the number of levels in output voltage will try to match the sine waveform. It infers that increase that multilevel conversion reduces harmonic distortion at the inverter output. In addition the switching losses get reduced by decreased the carrier frequencies of the inverter, this can be achieved by controlling the slope of the carrier signals. Such modulation techniques are Phase Disposition (PD), Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD), Carrier Overlapping (COPWM) and Inverted Sine (IS PWM) [9], [10]. This paper proposes a new three-phase seven-level Reverse voltage multilevel inverter (RVMLI) with less number of switches and voltage sources. In this topology, current flows from load to source. So the voltage component also reversed. So this topology is called Reverse Voltage MLI [8]. PD PWM (Phase Disposition Pulse Width Modulation), APOD PWM (Alternate Phase Disposition Pulse Width Modulation), CO PWM (Carrier Overlapping Pulse Width Modulation) and IS PWM (Inverted Sine Pulse

Width Modulation) control techniques are used to control the proposed the proposed multilevel inverter topology.

2 circuit diagram

Fig.1 shows schematic of single phase seven-level inverter. This topology is a hybrid multilevel inverter topology which separates the output voltage levels into two units. One unit is level generation unit which is used to produce output voltage levels in positive polarity. This part uses high-frequency switches operating at 2 kHz frequency. The other unit is called polarity generation unit which is used to produce output voltage with required polarity. This part uses low frequency switches operating at line frequency (50Hz).

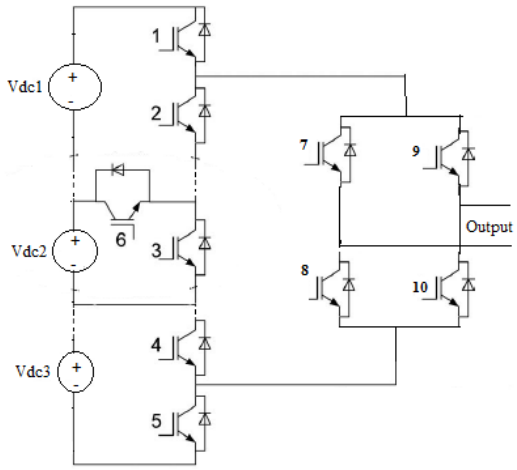

Fig.1. Reverse Voltage MLI circuit

Fig. 2 shows schematics of three-phase seven-level inverter topology. In this, eighteen high frequency switches are used which are used to generate required output voltage levels and twelve low frequency switches are used which are used to generate output voltage with required polarity.

Switching sequences for level and polarity generation unit for single phase RV MLI is shown in table 1. In this table, 1 indicates that the corresponding switch will be turned ON and 0 indicates the OFF state.

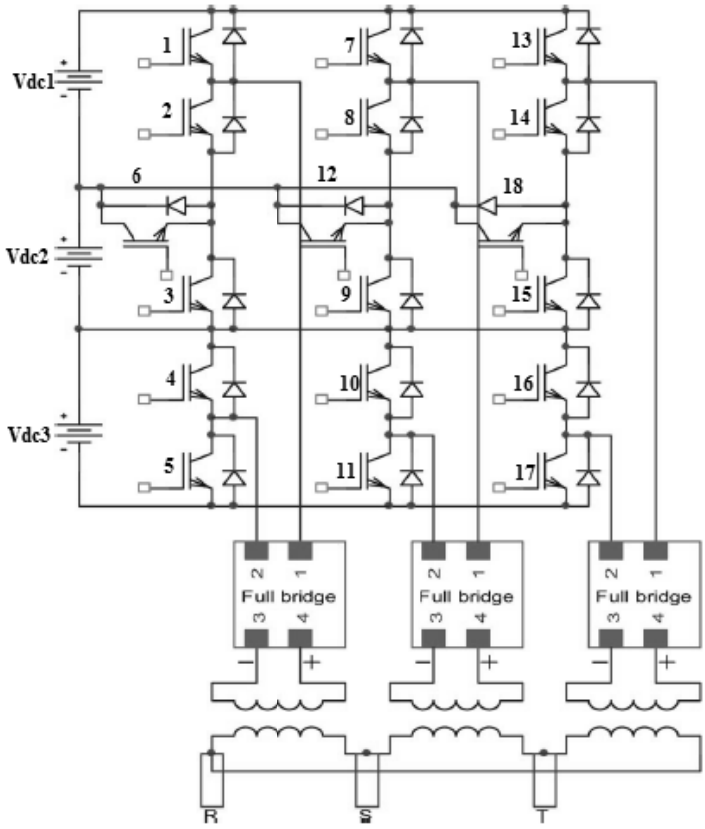

Fig.2. Three-phase Reverse Voltage MLI circuit

TABLE 1 SWITCHING SEQUENCES FOR SINGLE PHASE SEVEN-LEVEL INVERTER

Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
1	0	1	1	1	0	0	0	1	1	0
2	0	1	1	0	1	0	0	1	1	0
3	1	0	0	1	0	1	0	1	1	0
4	1	0	0	0	1	0	0	1	1	0
5	0	1	1	1	0	0	1	0	0	1
6	0	1	0	1	0	1	1	0	0	1
7	0	1	0	0	1	1	1	0	0	1
8	1	0	0	0	1	0	1	0	0	1

3 VARIOUS PWM CONTROL TECHNIQUES

3.1 CO PWM

Three carriers generated for three phase seven-level is overlapped each other. So it is called Carrier Overlapping Pulse Width Modulation (COPWM) technique. In this, amplitude modulation index is one. If the sinusoidal signal is greater than a carrier signal (triangular waveform), then the active device corresponding to that carrier is switched on and if the reference signal is less than a carrier waveform, then the active device corresponding to that carrier is switched off.

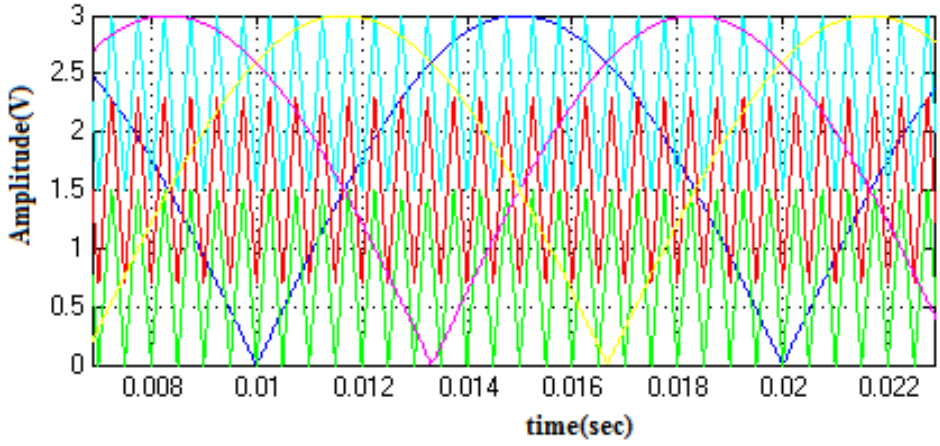

Fig.3. CO PWM waveform

3.2 ISPWM

In this, carrier wave is inverted sine wave i.e. sine wave is shifted by 180degree. So this pulse width modulation technique is called Inverted Sine PWM. In this, (N-1)/2 carriers are used. N is the number of output voltage levels.

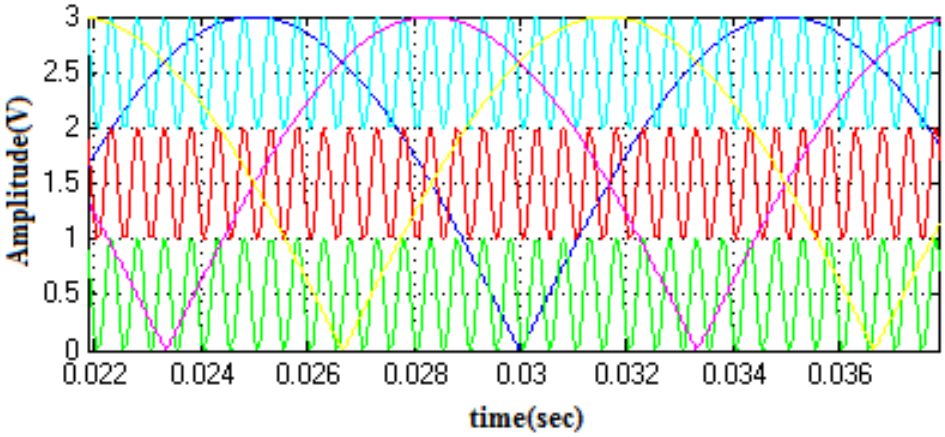

Fig.4. IS PWM waveform

3.3 APOD PWM

In this technique, carrier signal (triangular wave) is in out of phase with its neighbor carrier waveform by 180 degree. When the number of levels N = 7, there are (N – 1)/2 = 3 carrier signals arranged so that every carrier signal is in out of phase with its neighbor carrier by 180 degree.

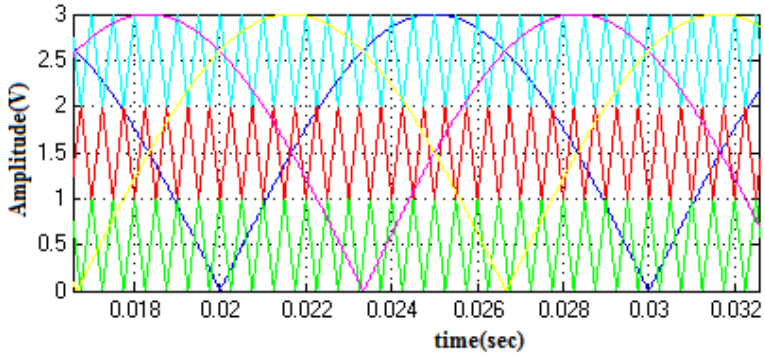

Fig.5. APOD PWM waveform

3.4 PD PWM

Fig. 6 shows the carrier arrangements for PDPWM control strategy ma=1 for a seven level inverter to be in phase from each other. There are six distinct carriers, all in phase with one another and with the same amplitude *Ac.*

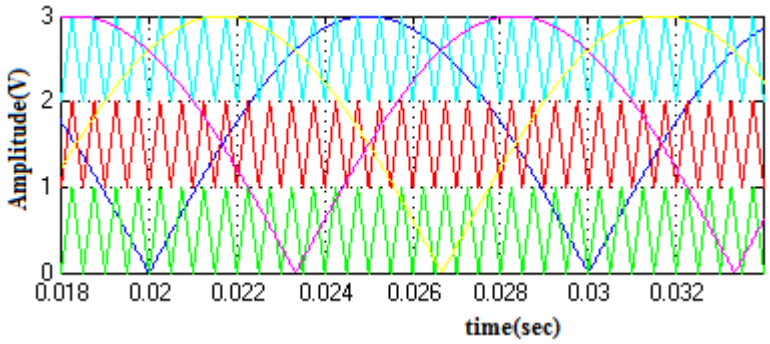

Fig.6. PD PWM waveform

4 SIMULATION RESULTS

The following parameter values are used for simulation: Vdc1 =10V, Vdc2 =10V and Vdc3 =10V for each phase.

Three-phase seven-level proposed inverter output voltage waveform by using various PWM control techniques like COPWM, ISPWM, APOD & PD PWM is shown in fig.7, 8,9 and 10.

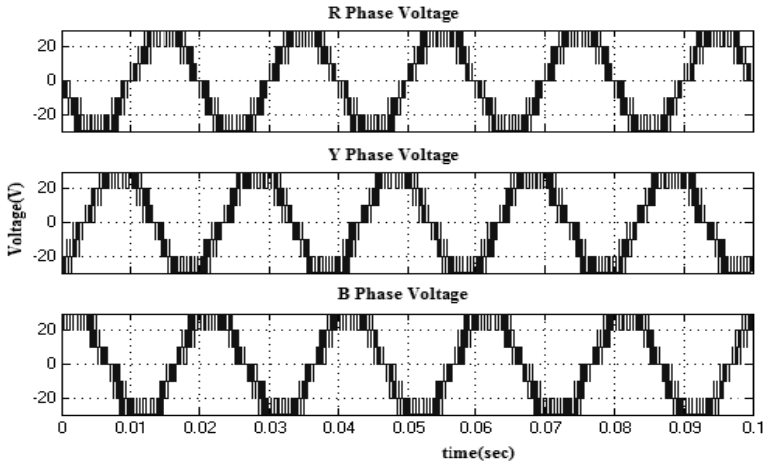

Fig.7. Output Voltage generated by CO PWM control strategy

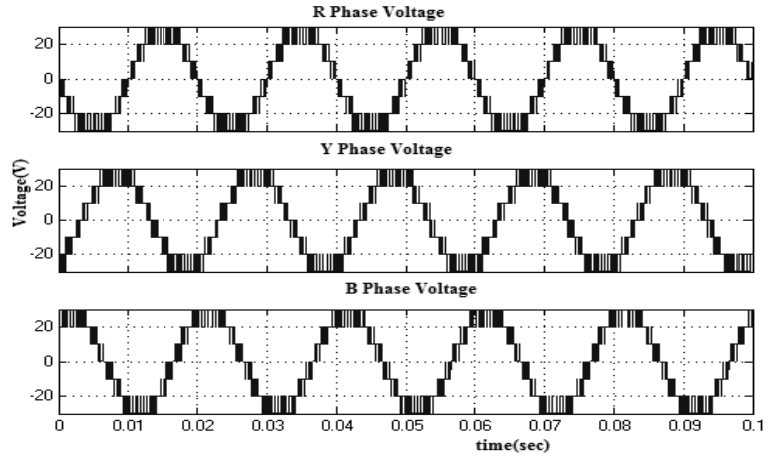

Fig.8. Output Voltage generated by IS PWM control strategy

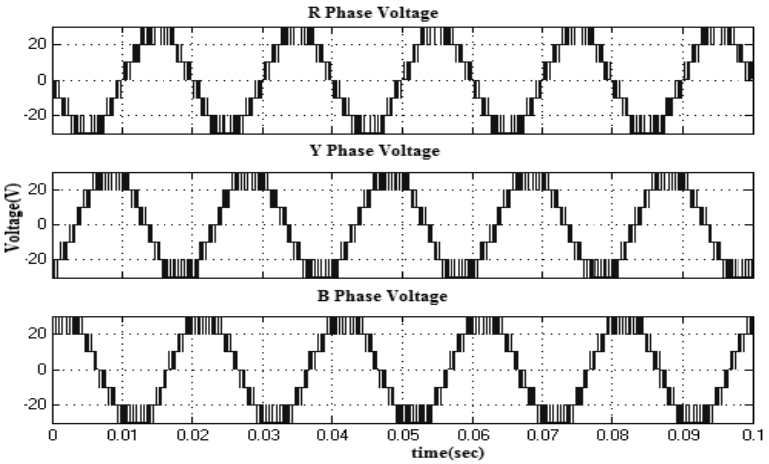

Fig.9. Output Voltage generated by APOD PWM control strategy

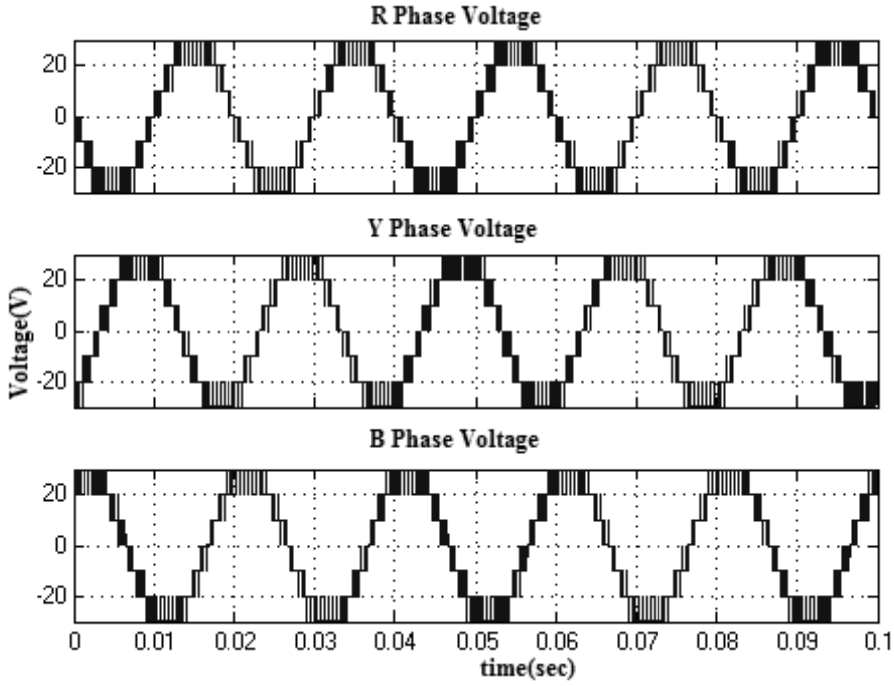

Fig.10. Output Voltage generated by PD PWM control strategy

Output Voltage Harmonic Distortion by using COPWM control strategy is 23.30% and the fundamental is 30.02 V.

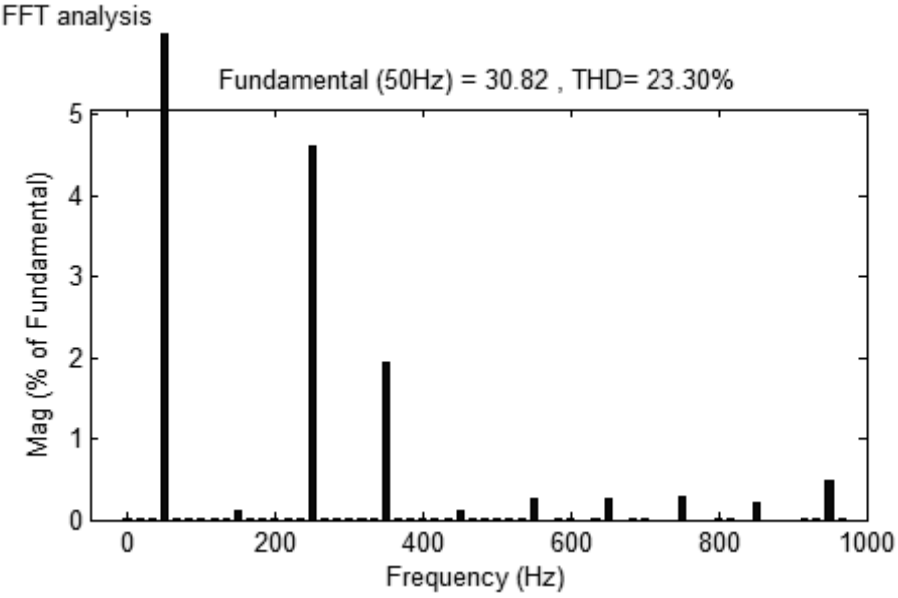

Fig.11. Harmonic Spectrum with m_a=1 by using COPWM control technique

Output Voltage Harmonic Distortion by using ISPWM control strategy is 19.81% and the fundamental is 29.63 V.

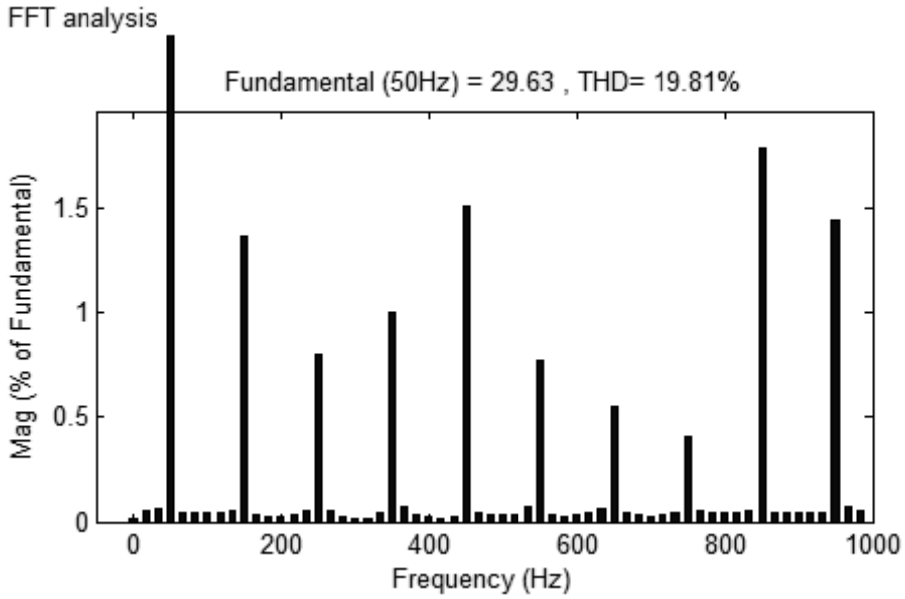

Fig.12. Harmonic Spectrum with m_a=1 by using IS PWM control technique

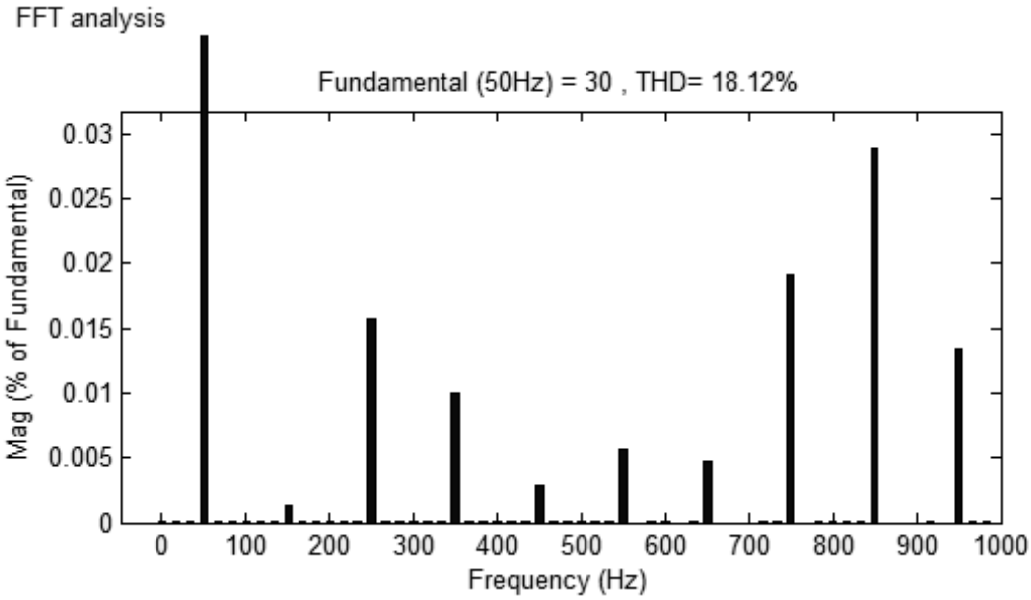

Fig.13. Harmonic Spectrum with m_a =1 by using APOD PWM control technique

Output Voltage Harmonic Distortion by using APOD PWM control strategy is 18.12% and the fundamental is 30V.

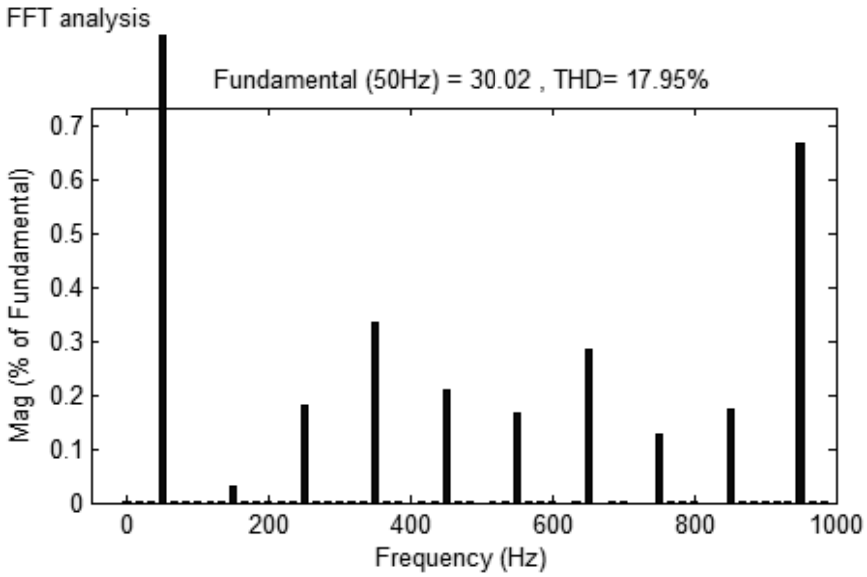

Fig.14. Harmonic Spectrum with m_a =1 by using APOD PWM control technique

Output Voltage Harmonic Distortion by using COPWM control strategy is 17.95% and the fundamental is 30.02

Table 2, 3, 4 and 5 shows variation of Total Harmonic Distortion (THD), peak value of output voltage, RMS voltage and Crest Factor for different PWM techniques with various modulation indexes.

Table 6 shows variation of Total Harmonic Distortion (THD) of output current for different PWM techniques with various modulation indexes and the corresponding graph is shown in fig.16.

TABLE 2 %THD OF OUTPUT VOLTAGE OF RVMLI FOR VARIOUS VALUES OF M_A

m_a	**COPWM**	**ISPWM**	**APOD**	**PDPWM**
1	23.3	19.81	18.12	17.95
0.97	24.92	21.48	20.22	19.74
0.93	26.56	22.53	21.73	21.07
0.9	28.02	23.29	22.74	22.15
0.87	29.71	24.27	23.5	22.98

TABLE 3 PEAK (FUNDAMENTAL) VALUES OF OUTPUT VOLTAGE OF RVMLI FOR DIFFERENT PWM STRATEGIES AND VARIOUS VALUES OF M_A

m_a	COPWM	ISPWM	APOD	PDPWM
1	30.82	29.63	30	30
0.97	29.99	28.51	29	28.98
0.93	29.12	27.72	28	27.97
0.9	28.26	26.93	27	27.04
0.87	27.3	26.13	26	26.07

TABLE 4 RMS (FUNDAMENTAL) VALUES OF OUTPUT VOLTAGE OF RVMLI FOR DIFFERENT PWM STRATEGIES AND VARIOUS VALUES OF M_A

m_a	COPWM	ISPWM	APOD	PDPWM
1	21.8	20.95	21.21	21.23
0.97	21.2	20.16	20.51	20.49
0.93	20.59	19.6	19.8	19.78
0.9	19.98	19.04	19.09	19.12
0.87	19.31	18.48	18.38	18.44

TABLE 5 CREST FACTOR OF OUTPUT VOLTAGE OF RVMLI FOR DIFFERENT PWM STRATEGIES AND VARIOUS VALUES OF M_A

m_a	COPWM	ISPWM	APOD	PDPWM
1	1.414	1.414	1.4144	1.4131
0.97	1.4146	1.4142	1.414	1.4143
0.93	1.414	1.4143	1.4141	1.4141
0.9	1.4144	1.4144	1.4144	1.4142
0.87	1.414	1.414	1.4146	1.414

TABLE 6 %THD (FUNDAMENTAL) OF OUTPUT CURRENT OF RVMLI FOR VARIOUS VALUES OF M_A

m_a	COPWM	ISPWM	APOD	PDPWM
1	2.6	0.58	0.13	0.19
0.97	2.57	0.8	0.14	0.23
0.93	2.53	0.82	0.15	0.22
0.9	2.5	0.91	0.16	0.3
0.87	2.37	0.7	0.17	0.41

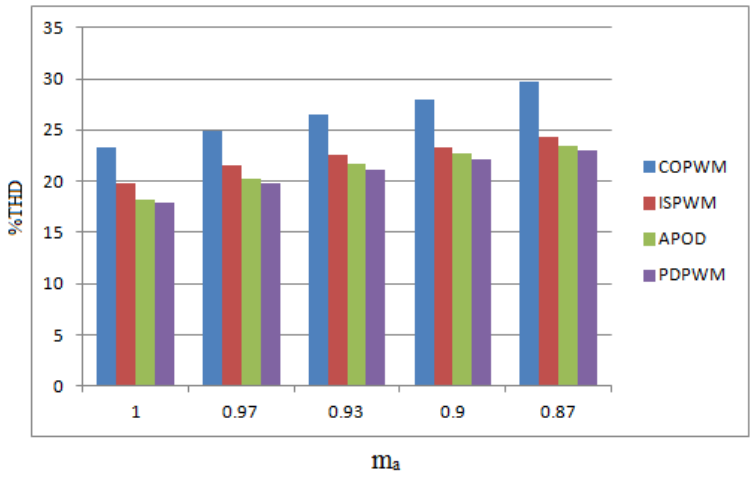

Fig.15. Graph for voltage THD vs m_a

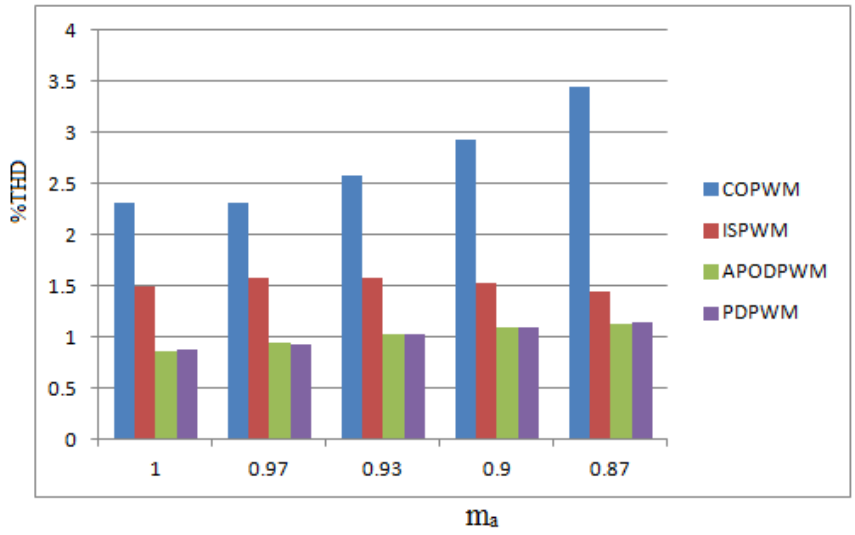

Fig.16. Graph for current THD vs m_a

5 CONCLUSION

A three phase seven-level Reverse Voltage multilevel inverter topology has been presented and simulated by using MATLAB/Simulink. Various Pulse Width Modulation (PWM) control techniques like COPWM, ISPWM, PDPWM, APOD PWM control strategies are developed with different amplitude modulation indexes. The variation of Total Harmonic Distortion (THD) in the output voltage and current is measured. It is observed that PDPWM control technique produces less THD in the output voltage and current.

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