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A Modified Cascaded H-Bridge Multilevel Inverter topology with Reduced Number of Power Electronic Switching Components

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Abstract

This paper presents a seven level Cascaded H-Bridge Multilevel Inverter based on a Multilevel DC Link (MLDCL) topology and a single full bridge inverter to reduce the number of power electronic switching devices required by its conventional counterpart. Normally, Inverter produces square wave ac output and so it is called as two-level inverter. Compared to two-level inverter, Multilevel Inverters (MLI's) are having high efficiency since they produce accurate sinusoidal (staircase) output. Cascaded H-bridge multilevel inverter consists of separate full bridge inverters which are connected to individual dc sources for producing different levels in the output voltage. This type is advantageous because, it does not require additional clamping diodes and balancing capacitors as in the case of diode-clamped and flying capacitor types respectively. The Unique feature of MLI is , "the more the number of output voltage levels ,the less the harmonic content in it". But, if the number of output voltage level is increased, it requires more number of switches which leads to circuit complexity. Therefore, the Proposed topology introduces a Multilevel D.C link using half bridge cells connected to separate dc sources which produces a staircase dc voltage and a single H-Bridge inverter to invert that dc voltage to staircase ac output. Thus, the MLDCL inverter significantly reduces the switch count. Multi-Carrier based Pulse Width Modulation technique is used to operate the switching devices in such a manner so as to achieve good fundamental output voltage with low switching losses. MATLAB/SIMULINK is used to verify the performance of the proposed model.

Keywords: Multilevel Inverter, Cascaded H-Bridge, Multilevel DC link, Staircase output, Pulse Width Modulation,Total Harmonic Distortion.

Introduction

Normally, Inverters are used to convert dc input (e.g: from PV cells) to ac output. Inverters are mainly classified into, two level Inverter and Multilevel Inverter. The voltage source inverters produce an output voltage or current with levels either '0' or '$\pm V_{dc}$' (square wave output). They are known as two-level inverters. To produce a quality output voltage or current waveform with less amount of ripple content, they require high switching frequency along with various pulse width modulation (PWM) strategies. In high power and high voltage applications, these two level inverters, however, have some limitations in operating at high frequency mainly due to switching losses and constraints of device ratings. Moreover, the semiconductor switching devices should be used in such a manner as to avoid problems associated with their series-parallel combinations that are necessary to obtain capability of handling high voltages and currents.

The recent advancement in power electronics has initiated to improve the level of inverter to satisfy the need of medium voltage high power applications without the need of transformer which leads to the invention of multilevel inverters [11]. These inverter topologies can generate high quality voltage waveforms with power semiconductor switches operating at a frequency near the fundamental. It significantly reduces the harmonics problem with reduced voltage stresses across the switch. These limitations can be overcome by using multilevel inverters. Compared to 2-level inverters, Multilevel inverters are having high efficiency since it produce accurate sinusoidal (staircase) output using different levels in the output voltage. This paper focuses on Cascaded H-Bridge type Multilevel inverter which is advantageous than other two types.

Cascaded H Bridge (CHB) multilevel inverter is one of the most important topologies in the family of multilevel and multi pulse inverters. It is built to synthesize a desired AC voltage from several levels of DC voltages. CHB is simpler than diode clamped and flying capacitor MLI topologies because of some advantages such as automatic voltage sharing, smaller dv/dt stresses, switching redundancy and requirement of least number of components, no high rated capacitors and diodes and circuit layout flexibility [7]. It consists of a series or cascade connection of several single phase full bridge inverter units with respect to the number of output voltage levels to produce sinusoidal AC output. The concept of multilevel inverters is that, if the number of voltage levels is increased, then the harmonic content in the output voltage gets reduced and so, the number of active switches also increased. This leads to more number of switches and their gate circuits which increases the circuit complexity. This paper focuses to reduce the required number of active switches by providing a multilevel DC link (MLDCL) instead of each full bridge inverter units in the CHB topology [10].

A power electronic multilevel inverter is essentially a device for creating a variable AC Magnitude and Frequency output from a DC input. However the variable frequency ability is nearly always accompanied by a corresponding need to adjust the

amplitude of fundamental component of the output waveform as the frequency changes, i.e., voltage control. One of the most widely utilized strategies for controlling the AC output of power electronic converters is the technique known as pulse width modulation (PWM). This varies the duty cycle of the inverter switches at a high frequency to achieve an average low- frequency output voltage or current [6]. Several developments of PWM concept addressing the main objectives of reduced harmonic distortion and increased output magnitudes for a given switching frequency and the development of modulation strategies to suit different inverter topologies. A multicarrier based PWM technique is proposed in this paper. In this technique, the sinusoidal reference waveform of each phase and a periodic triangular carrier wave are compared and the intersection points determine the commutation instants of the associated inverter leg switches.

Multilevel Inverters

Multilevel inverters have drawn tremendous interest in the power industry. They present a new set of features that are well suited for use in reactive power compensation. It may be easier to produce a high-power, high voltage inverter with the multi level structure because of the way in which the device voltage stresses are controlled in the structure. Increasing the number of voltage levels in the inverter without requiring higher ratings on individual devices can increase the power rating .The unique structure of multilevel voltage source inverter allows them to reach high voltages with low harmonics without the use of transformers or series connected synchronized switching devices. As the number of voltage levels increases, the harmonic content of the output voltage waveform decreases significantly.

The general structure of the multilevel inverter is to synthesize a near sinusoidal voltage from several levels of dc voltages, typically obtained from capacitor voltage sources [11]. As the number of levels increases, the synthesized output waveform has more steps, which produce a staircase wave that approaches a desired waveform. Also, as more steps are added to the waveform, the harmonic distortion of the output waveform decreases, approaching zero as the number of levels increases [2]. As the number of levels increases, the voltage that can be spanned by summing multiple voltage levels also increases. The advantages of Multilevel Inverters are they offer a low output voltage THD and a high efficiency and power factor. They are suitable for high voltage and high current applications [11]. They have higher efficiency because the devices can be switched at a low frequency. They do not suffer from Electromagnetic Interference (EMI) problems. Multilevel inverters are mainly classified into three types namely, Diode clamped type, flying capacitor type, Cascaded H-Bridge type.

Cascaded H-Bridge Multilevel Inverter

The last structure is a multilevel inverter, which uses cascaded inverters with separate dc sources (SDCSs).The general function of this multilevel inverter is the same as that of the other two inverters. The multilevel inverter using cascaded inverter with

SDCSs synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from solar cells [5]. This configuration recently becomes very popular in ac power supply and adjustable speed drive applications. This new inverter can avoid extra clamping diodes or voltage balancing capacitors.

The main features of CHBMLI are, for real power conversions from ac to dc and then dc to ac, the cascaded inverter needs separate dc sources. The structure of separate dc sources is well suited for renewable energy sources such as fuel cell, photovoltaic and biomass [7]. Compared with the diode clamped and flying capacitor types, it requires the least number of components to achieve the same number of voltage levels. Soft switching techniques can be used to reduce switching losses and device stresses

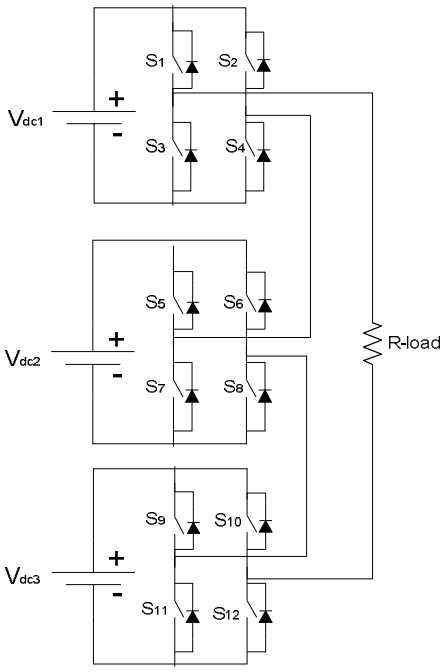

Figure 1: Circuit Diagram of Conventional CHB MLI.

For producing seven level output voltage, the CHBMLI requires three single phase full bridge inverters which are connected in series as shown in its circuit diagram in figure 1. These three inverter bridges are connected to three independent dc sources which are having equal amplitude and therefore it is called as SMLI (Symmetrical MLI). If the input dc sources are of different amplitudes, then it is called as ASMLI (Asymmetrical MLI) [2], [3].

In the case of seven level CHB inverter, the ac output voltage at each level can be obtained in the same as in normal 2 level manner. The AC terminal voltages of different level inverters are connected in series. During first mode of operation, by different combinations of the six switches S_1,S_4,S_5,S_8,S_9, and S_{12}, each inverter level

can generate four different voltage outputs V_{dc},$2V_{dc}$,$3V_{dc}$, and zero. The conduction of these switches leads to positive half cycle of the output voltage waveform with these three levels and zero level. During the second mode, through different combinations of switches S2, S_3, S_6, S_7, S_{10}, and $S_{11,}$ each inverter level can generate four different voltage outputs-V_{dc}, -$2V_{dc}$, -$3V_{dc}$, and zero which leads to the negative half cycle of the output voltage waveform. The ac output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs [7].Thus, a seven level output voltage of V_{dc},$2V_{dc}$, $3V_{dc,}$ -V_{dc}, -$2V_{dc}$, -$3V_{dc}$, and a zero level can be obtained as shown in figure 2. through this proper switching operation.

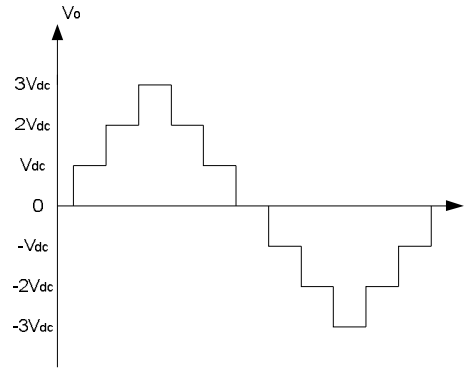

Figure 2: Output voltage waveform of 7-level CHBMLI

In this topology, the number of output phase voltage levels is defined by m = 2s+1, where s is the number of dc sources. This conventional 7-Level CHBMLI requires 2(m-1) = 2(7-1) = 12 switches. The main advantage of this CHBMLI topology is that the Total Harmonic Distortion (THD) present in the output voltage gets decreased if the number of output voltage level is increased greatly. But, there is a difficulty to achieve this, that is, it requires more number of switching devices to generate more number of levels. This leads to circuit complexity and more cost. A better solution to this problem is Multi Level DC Link (MLDCL) topology which is proposed in this paper.

Proposed Multilevel Dc Link (MLDCL) Inverter

The circuit diagram of the proposed 7-level Cascaded H-bridge MLDCL inverter topology is shown below in figure 3, which consists of a multilevel DC source to produce DC-link bus voltage V_{bus} and a single-phase full-bridge (SPFB) inverter consists of four switches S7-S10 to invert the polarity of the DC-link bus voltage to produce an AC voltage [10].

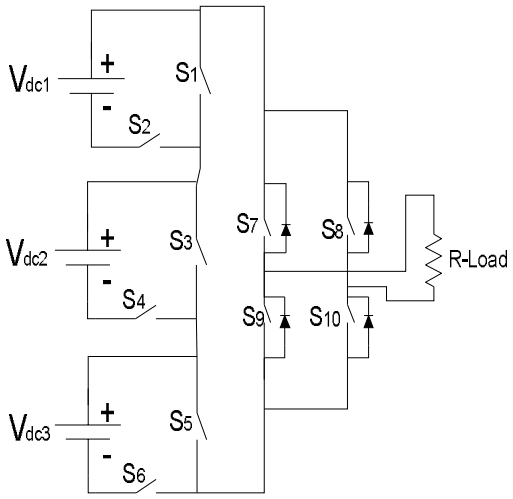

Figure 3: Circuit Diagram of Proposed MLDCL inverter

The DC source is formed by connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two switches. These two switches operate in a toggle fashion. Low on resistance and fast switching capability, low voltage switches are utilized in each cell source to reduce the inverter cost or to provide a high bandwidth sinusoidal output voltage. These switches are triggered by proper switching signals which are obtained by using suitable PWM technique in order to produce multilevel output voltage.

Table I. Comparison of Multilevel Inverters

Converter Type	**Diode Clamped**	**Flying Capacitor**	**Cascaded H-Bridge**	**Proposed MLDCL**
Main Switches	(m-1)*2	(m-1)*2	(m-1)*2	m+3
Main Diodes	(m-1)*2	(m-1)*2	(m-1)*2	m+3
Clamping Diodes	(m-1)*(m-2)	0	0	0
Balancing Capacitors	0	(m-1)*(m-2)/2	0	0

From Table I, when compared with the existing multi level inverters, the new MLDCL inverters can significantly reduce the switch count as well as the no of gate drivers as the no of voltage levels increases. Also, it does not require additional clamping diodes and balancing capacitors as in the case of DCML and FCML type inverters [13]. So, it can be seen that roughly half the number of components can be eliminated as ‘m’ increases. In this paper, the conventional 7-level CHBMLI requires

(m-1)*2 = (7-1)*2 = 12 switching devices. But, the proposed CHB MLDCL inverter requires only (m+3) = (7+3) =10 switches [2], [10]. Therefore, this proposed type is more advantageous since the number of switching devices is greatly decreased from (m-1)*2 (conventional) to m+3 (MLDCLI) even if the number of levels of output voltage is increased [1], [10].

To obtain high quality ac output, the value of THD should be minimum. To minimize the THD; the number of levels should be increased [9]. For that, this Proposed MLDCL inverter is more feasible and cheaper than the other types. The switching device may be any of the power semiconductor switching devices like power diodes, thyristors, Bipolar junction transistors (BJTs), power metal oxide semiconductor field effect transistors (MOSFETs) and Insulated gate bipolar transistors (IGBTs).

In this case, IGBT acts as a switching device. An IGBT combines the advantages of BJT and MOSFET. An IGBT has high input impedance like MOSFET and low on-state conduction losses like BJT. However, there is no secondary breakdown problem as with BJTs. An IGBT is turned on by just applying a positive gate voltage and is turned off by removing the gate voltage. It requires a very simple driver circuit. It has lower switching and conducting losses while sharing many of the appealing features of power MOSFETs such as ease of gate drive, peak current, capability and ruggedness. IGBTs are finding increasing applications in medium power applications such as dc and ac motor drives, power supplies, solid state relays and contactors [11]. As the upper limits of commercially available IGBT ratings are increasing, they are finding and replacing applications where BJTs and conventional MOSFETs were predominantly used as switches. Through proper modulation techniques, the gate pulse to the IGBT is obtained and operating the IGBT switch in such a way to produce accurate sinusoidal (step) output voltage waveform with less THD.

Pulse Width Modulation

It is generally accepted that the performance of an inverter with any switching strategies, can be related to the harmonic contents of its output voltage. Power electronics researchers have always studied many novel control techniques to reduce harmonics in such waveforms. Up-to-date, there are many techniques, which are applied to inverter topologies [11]. One of the mostly widely utilized strategies for controlling the AC output of power electronic converters is the technique known as pulse width modulation (PWM) [8]. This varies the duty cycle of the inverter switches at a high frequency to achieve a target average low- frequency output voltage or current. Similar to two-level inverters, there are also different types of modulation techniques adopted for multilevel inverters.

Sinusoidal pulse width modulation (SPWM) is one of the primitive techniques, which are used to suppress harmonics presented in the quasi-square wave. In this method, the sinusoidal reference waveform of each phase and a periodic

triangular carrier wave are compared and the intersection points determine the commutation instants of the associated inverter leg switches [6]. In multilevel case, SPWM technique uses carrier disposition PWM (CDPWM) where modulation is achieved by having m-1 triangular carriers where m is the number of voltage levels. These carriers are arranged so that they fully occupy continuous bands in the range of $-(m-1)V_{dc}/2$ to $(m-1)V_{dc}/2$. A single sinusoidal reference is then compared with these carriers to determine the switched voltage level. Therefore, for our 7-level CHBMLI, 6 triangular carriers are required which occupy the continuous bands in the range of $-3V_{dc}$ to $+3V_{dc}$.The degree of freedom for this CDPWM technique is,

$$M_a = \frac{2\times A_r}{(m-1)\times A_c} \quad (1)$$

Where,

'A_r'represents the reference waveform amplitude.
'A_c'represents the carrier waveform amplitude.
'm' denotes the number of levels.

This CDPWM strategy includes three types with three differently disposed triangular carriers which are,

1) Alternate phase disposition (APD) – every carrier waveform is in out of phase with its neighbor carrier by 180°.
2) Phase opposition disposition (POD) – All carrier waveforms above zero reference are in phase and are 180° out of phase with those below zero.
3) Phase disposition (PD)-All carrier waveforms are in phase.

This paper is focused only on the third type (PD).

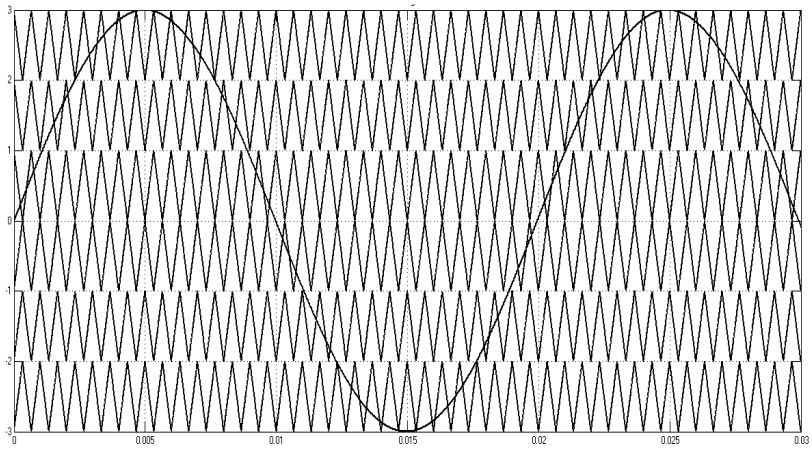

Figure 4: PDPWM technique for 7-level CHBMLI

Figure 4. shows that a single sinusoidal reference waveform is compared with periodic triangular carrier waves and the intersection points determine the ON and OFF pulse durations for the switches [6].

Results and Discussion

The implementation of the conventional circuit in MATLAB employing multicarrier based PWM technique is shown below in figure 5 and whose output voltage is simulated which is shown in figure 5.A.

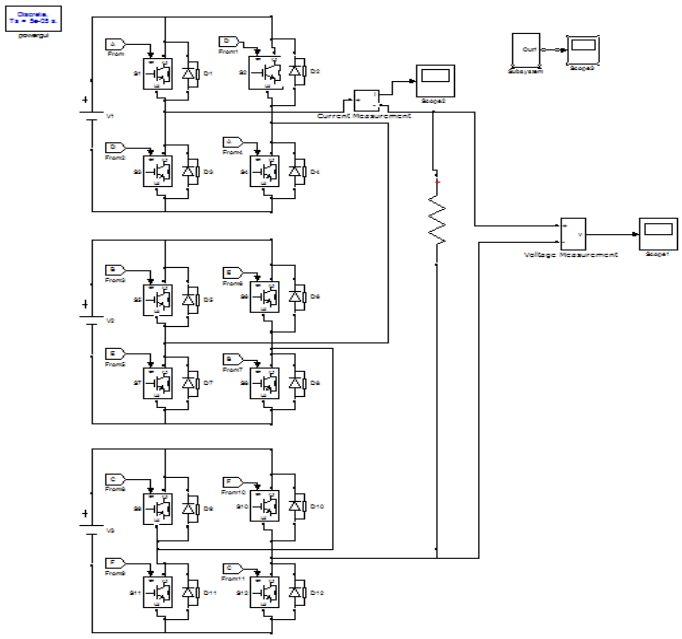

Figure 5. SIMULINK model for conventional 7-level CHBMLI

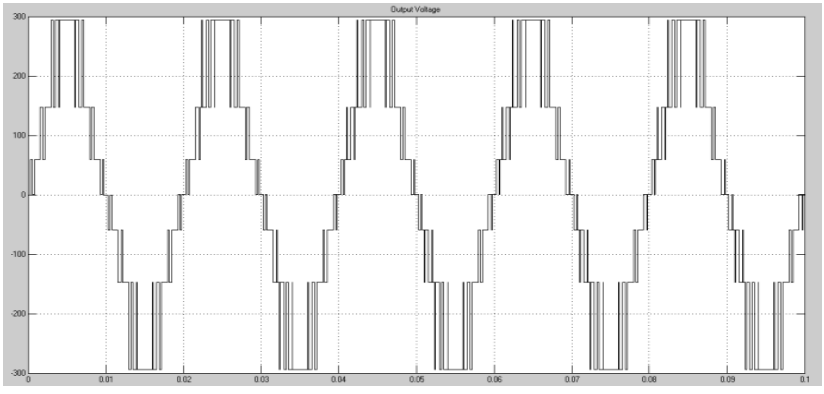

Figure 5.A. Output Voltage of conventional 7-levelCHBMLI

Likewise, the proposed circuit with less number of switches is simulated by creating a SIMULINK model as shown in figure 6.The subsystem model for performing multi carrier PWM is developed as shown in figure 6.A.

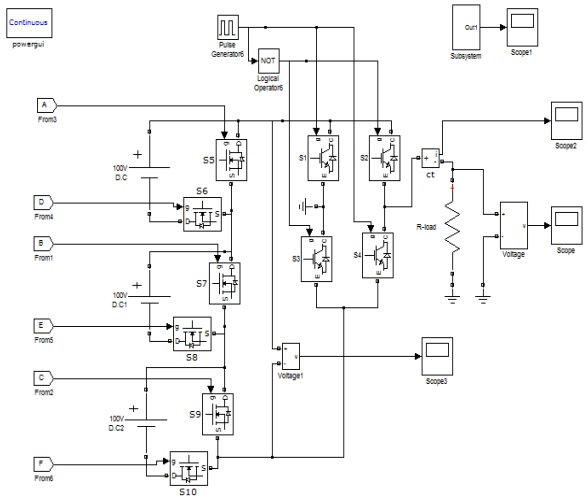

Figure 6. SIMULINK model for proposed CHB MLDCL Inverter

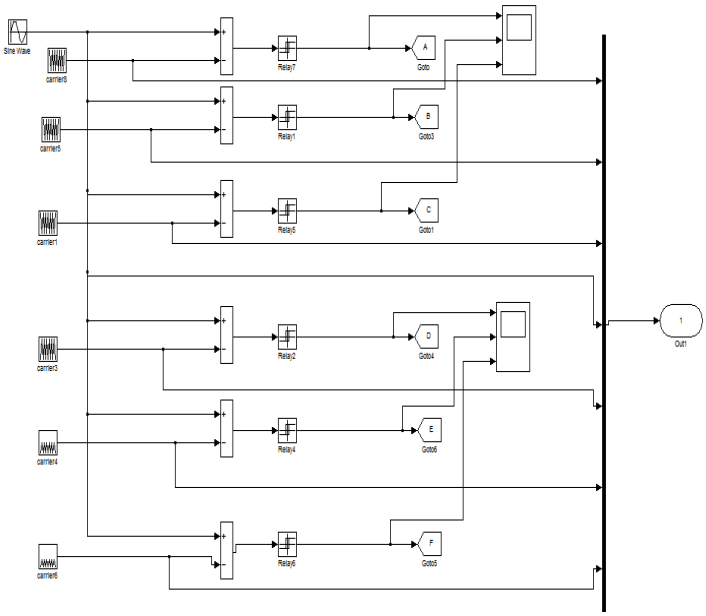

Figure 6.A. Subsystem model for gate pulse generation

The subsystem model as shown in figure 6.A. performs pulse width modulation using multiple triangular carriers and produces necessary pulses for the switches with different ON and OFF durations depending upon the intersection points. The pulses generated from the subsystem model are shown below in figures 6.B and 6.C for the switches which are going to conduct in positive and negative half cycles respectively.

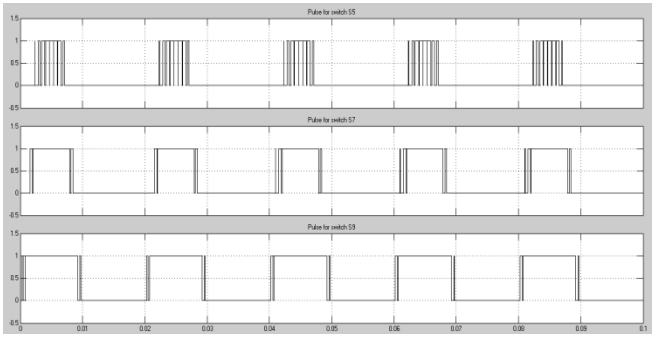

Figure 6.B. Pulses for positive half switches

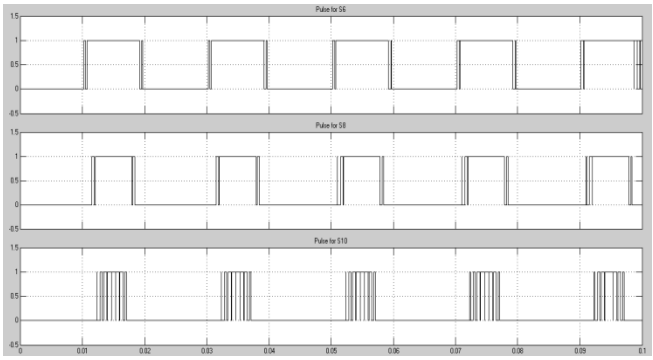

Figure 6.C Pulses for Negative half switches

In response to these pulses, the switches conduct for different pulse durations and produce multilevel staircase output voltage as shown below in figure 6.D.

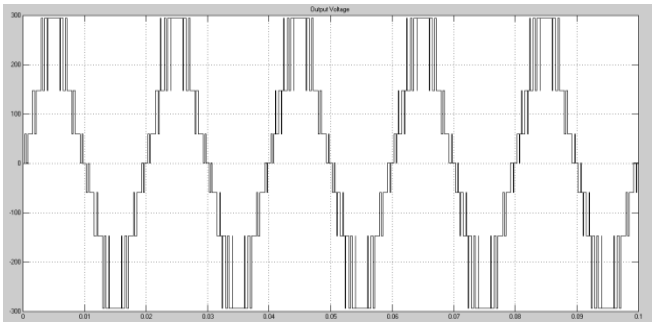

Figure 6.D Output Voltage of proposed MLDCL Inverter

The harmonics present in the output voltage can be analyzed in terms of Total Harmonic Distortion (THD) by performing Fast Fourier Transform (FFT) analysis using MATLAB. The FFT harmonic spectrum for output voltage indicating the THD in them is shown in figure 6.E.

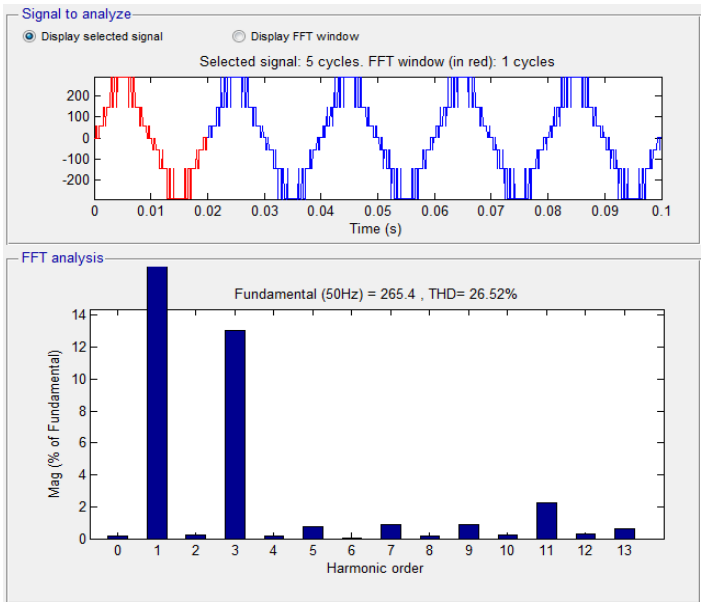

Figure 6.E. FFT spectrum of output voltage

From the FFT spectrum of output voltage, it is concluded that the value of THD is 26.52% without any filter circuit. The THD can be minimized greatly if the number of output voltage level is further increased to a large value [9].

Conclusion

Both the conventional 7-Level CHBML inverter and the proposed cascaded H-bridge MLDCL topology was simulated and it is concluded that for producing the same 7-level output voltage, the proposed MLDCL inverter requires only 10 switches whereas the conventional type requires 12 switches. This difference will be larger if the number of output voltage level is further increased. Therefore, the proposed cascaded H-bridge MLDCL topology can eliminate roughly half the number of switches, their gate drivers compared with the existing cascaded MLI counterparts. Despite a higher total VA rating of the switches, the cascaded MLDCL inverters are cost less due to the savings from the eliminated gate drivers.

This paper can be developed by interfacing renewable energy resources for providing DC supply to the proposed inverter circuit. Solar cells, Wind Energy generators, Fuel cells, etc can be interfaced with this MLDCL inverter to obtain high efficiency and also with low cost.

References

[1] Javad Ebrahimi., Ebrahim babei, 2012, "A New Multilevel Converter Topology with Reduced Number of Power Electronic Components," IEEE Transactions on Industrial Electronics, pp 655-667.

[2] Mazhar Hussain, Md., Vishnu Prasad, M., Pattabhi Ram, R.N.D., 2012, "Comparison between Symmetrical and Asymmetrical Single Phase Seven Level Cascade H-Bridge Multilevel Inverter with PWM Topology," in IJMSE, pp. 16-20.

[3] Seyezhai, R., 2012, "A Comparative Study of Asymmetric and Symmetric Cascaded Multilevel Inverter Employing Variable Frequency carrier based PWM," IJETAE, pp. 230-236.

[4] Sujitha, N., Ramani, K., 2012, "A New Hybrid Cascaded H-Bridge Multilevel inverter-Performance Analysis," ICAESM, pp. 46-50.

[5] Chitra, M., Bharathi Dasan, S.G., 2011, "Analysis of Cascaded H Bridge Multilevel Inverters with Photovoltaic Arrays," in Proceedings of ICETECT, pp. 442-447.

[6] Madhusudhan, V., Maruthi Prasad, T., 2011, "Comparison of Single phase Cascaded and Multilevel DC link inverter with Pulse width modulation control methods," in SEISCON, pp. 229-235.

[7] Huang huiying, xueYabin, XinYibo, 2011, "Research on Control and Structure of the Cascaded Multilevel Inverters," IEEE.

[8] Geethalakshmi, B., Delhibabu, K., 2011, "An Advanced Modulation Technique for the Cascaded Multilevel Inverter Used As A Shunt Active Power Filter," IEEE.

[9] Jimenez, O.L., Vargas, R.A., Aguayo, J., Arau, J.E., Vela, G., Claudio, A., 2011, "THD in Cascade Multilevel Inverters Symmetric and Asymmetric," Electronics, Robotics and Automotive Mechanics Conference, pp. 289-295.

[10] Rokan Ali Ahmed, Mekhilef, S., Hew Wooi Ping, 2010, "New Multilevel inverter topology with minimum number of switches," in TENCON, pp. 1862-1866.

[11] Muhammed, H. Rashid, 2004, "Power Electronics, Devices, Circuits and Applications," Third Edition, Pearson Education, Chap. 9, pp. 406-430.