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Design of Digit Serial FIR Filter

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Abstract

In the last two decades, many efficient algorithms and architectures have been introduced for the design of low complexity bit-parallel multiple constant multiplications (MCM) operation which dominates the complexity of many digital signal processing systems. On the other hand, little attention has been given to the digit-serial MCM design that offers alternative low complexity MCM operations albeit at the cost of an increased delay. In this paper, we address the problem of optimizing the gate-level area in digit-serial MCM designs and introduce high-level synthesis algorithms, design architectures, and a computer aided design tool. Experimental results show the efficiency of the proposed optimization algorithms and of the digit-serial MCM architectures in the design of digit-serial MCM operations and finite impulse response filters.

1. Introduction

Finite impulse response (FIR) filters are widely used in digital signal processing applications due to their stability and linear phase characteristics. FIR filters have a large number of multiplications involved in the filter algorithm, which are usually implemented using fixed-point or integer number representations with the filter coefficients being represented by a finite number of bits. In hard-wired ASIC designs, multiplication operations are replaced by shift-and-add operations towards multiplier less FIR filter design. From a power perspective, the fewer the number of adders, the less power the filter will consume.

The most common approaches to the implementation of digital filtering algorithms are general purpose digital signal processing chips for audio applications, or special purpose digital filtering chips and application-specific integrated circuits (ASICs) for

higher rates. This project describes an approach to the implementation of digital filter algorithms on field programmable gate arrays (FPGAs). Recent advances in FPGA technology have enabled these devices to be applied to a variety of applications traditionally reserved for ASICs. FPGAs are well suited to data path designs, such as those encountered in digital filtering applications. The density of the new programmable devices is such that a nontrivial number of arithmetic operations such as those encountered in digital filtering may be implemented on a single device. The advantages of the FPGA approach to digital filter implementation include higher sampling rates than are available from traditional DSP chips, lower costs than an ASIC for moderate volume applications, and more flexibility than the alternate approaches

2. System Objective

The impulse response $h[n]$ can be calculated if we set $x[n] = \delta[n]$ in the above relation, where $\delta[n]$ is the Kronecker delta impulse. The impulse response for an FIR filter then becomes the set of coefficients b_n, as follows

$$h[n] - \sum_{i=0}^{N} b_i \delta[n-i] - b_n$$

for $n = 0$ to N.

i. Plateform, Tools & Techniques
ii. MATLAB 7.3 (R2006B)
iii. Aldec Active HDL
iv. Quartus II

3. Filter Realization

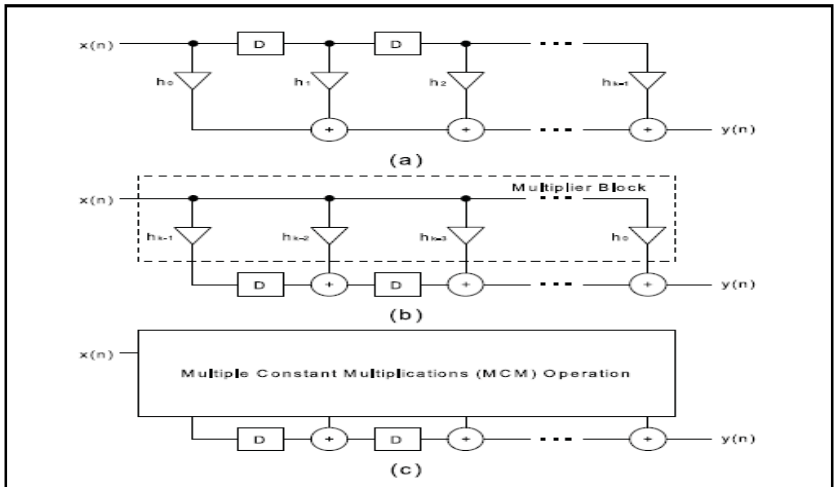

Fig. 5: FIR filters implementations(a) Direct form. (b) Transposed form with generic multipliers. *(c) Transposed form with an MCM block.*

The direct and transposed-form FIR filter implementations are illustrated in Fig. 5(a) and 5(b), respectively. The multiplier block of the digital FIR filter in its transposed form [Fig. 5(b)], where the multiplication of filter coefficients with the filter input is realized, has significant impact on the complexity and performance of the design because a large number of constant multiplications are required. This is generally known as the multiple constant multiplications (MCM) operation. The goal is the minimization of nonzero terms within the discrete coefficients as each nonzero term corresponds to an additional adder in the hardware implementation. Depending on the target hardware, it may be possible to implement a linear-phase FIR filter using less multipliers than the minimum-phase filter by taking advantage of the symmetry even if the filter length of the linear-phase is larger.

4. Design Implementation

In direct form structure even though there are only two multipliers, there are still three delays (same as for the direct-form structure) required since the number of delays corresponds to the order of the filter. The direct-form structure has the disadvantage that each adder has to wait for the previous adder to finish before it can compute its result. For high speed hardware such as FPGAs/ASICs, this introduces latency which limits how fast the filter can be clocked.

A solution to this is to use the transposed direct-form structure instead. With this structure, the delays between the adders can be used for pipelining purposes and therefore all additions/multiplications can be performed in fully parallel fashion. This allows real-time handling of data with very high sampling frequencies.

Direct Form Structure

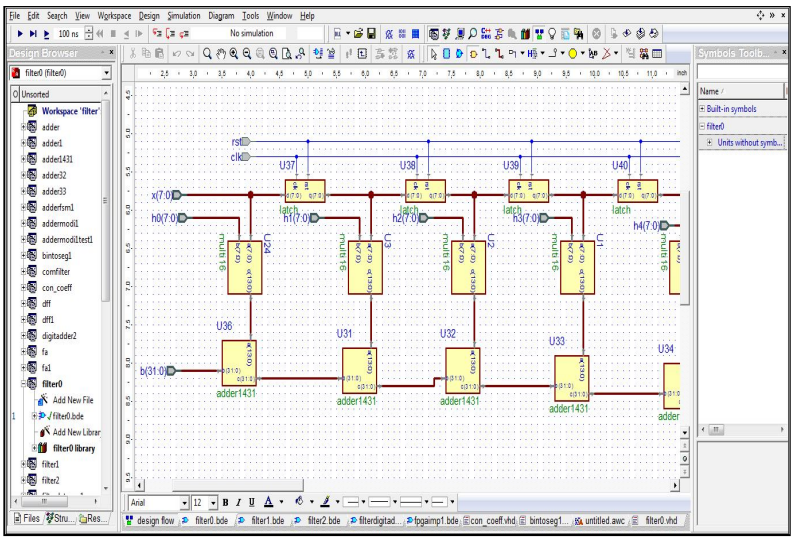

Fig. 1: Direct form of FIR filter.

1.2 Transpose form Structure

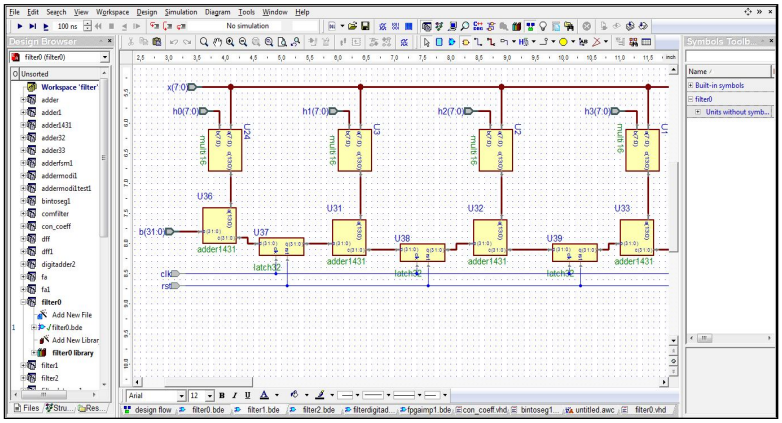

Fig. 2: Transpose form of FIR filter using Active HDL

1.3 Optimized Structure

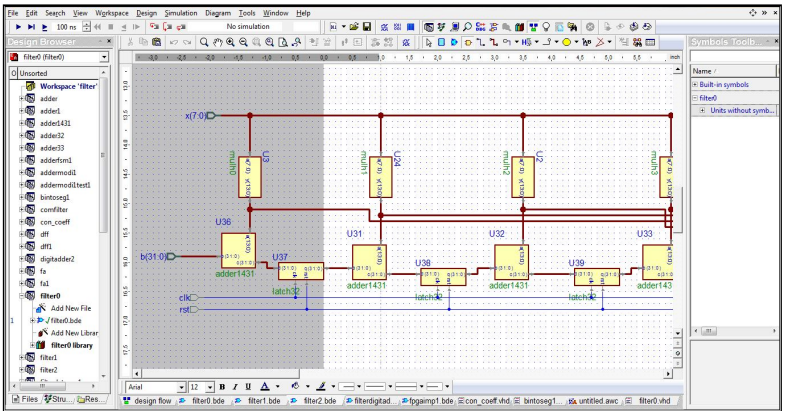

Fig. 3: Optimized Form of FIR filter using Active

Output Wave form of Filter 1 & Filter

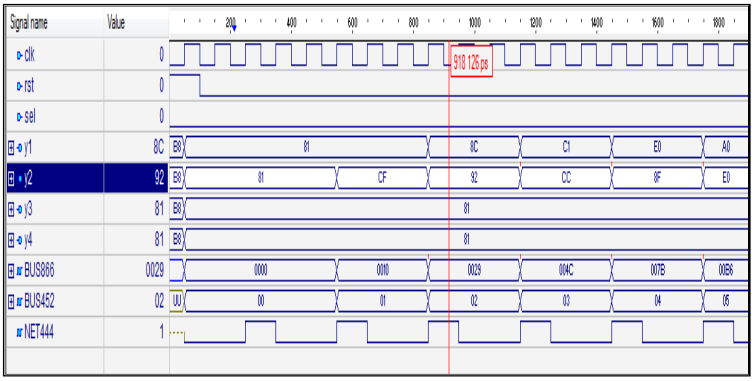

Fig. 4: Output Wave form of Filter 1 & Filter 2

Result Verification Through MATLAB

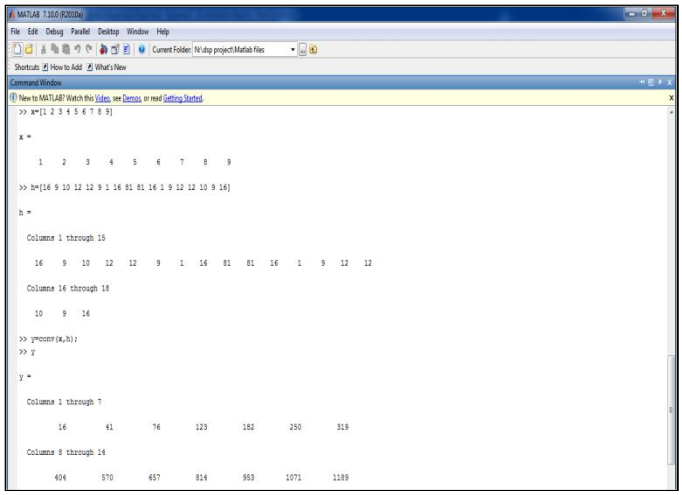

Fig. 5: Result Verification through MATLAB.

5. ARESULT

5.1 Compilation Report of Filter 1 and Filter 2

Table 1: Compilation Summary of Filter 1 and Filter 2

Specifications	Filter 1	Filter 2
Entity Name	Fpgaimp1	Fpgaimp2
Family	Cyclone	Cyclone
Device	EPIC6Q240C7	EPIC6Q240C7
Total logic elements	508/5980 (8%)	492/5980(8%)
Total Pins	51/185(28%)	20/185(11%)

Power Optimization Report of Filter 1 and Filter 2

Table 2: Power Comparison Of Filter 1 & Filter

Specification	Filter 1	Filter 2	Power Optimized
Total thermal Power dissipation	133.81 mW	104.44 Mw	21.949%
Core Dynamic thermal Power dissipation	7.87 mW	5.94 mW	24.523%
Core Static thermal Power dissipation	60.00 mW	60.00 mW	0
I/O thermal Power dissipation	65.94 mW	38.49 mW	41.628%

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