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Delay Reduction of CAM using Parity BIT

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Abstract

Content addressable memory (CAM) offers high speed search function in a single clock cycle. Because of parallel match line comparison CAM is power hungry hence we make use of high speed and low power ML sense amplifier. In this paper, with the introduction of parity bit in CAM its search delay is reduced by 39% with a little area and power overhead. Proposed design can work at a voltage of 5V.

INTRODUCTION

Most memory devices store and retrieve data by addressing specific memory locations. As a result, this path often becomes the limiting factor for systems that rely on fast memory accesses. The time required to find an item stored in memory can be reduced considerably if the item can be identified for access by its content rather than by its address. A memory that is accessed in this way is called content-addressable memory or CAM. Content addressable memory (CAM) is a type of solid-state memory in which data are accessed by their contents rather than physical locations. It receives input search data, i.e., a search word, and returns the address of a similar word that is stored in its data-bank. In general, a CAM has three operation modes: READ, WRITE, and COMPARE, among which “COMPARE” is the main operation as CAM rarely reads or writes. Figure. 1. shows the basic block diagram of Content Addressable Memory

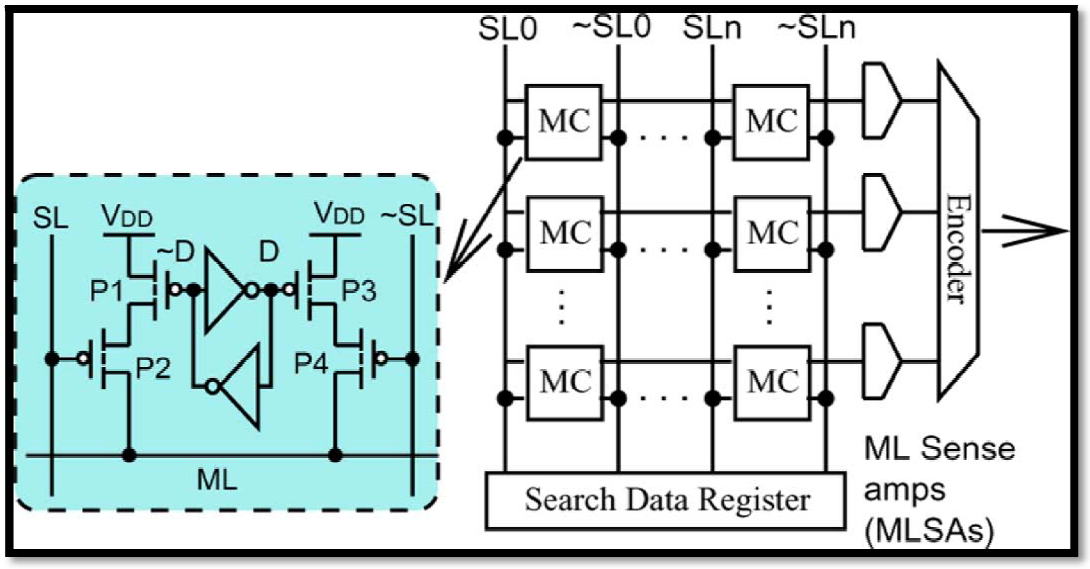

Figure. 1. 1. Block Diagram of Content Addressable Memory

In the simplified block diagram of a CAM core with an incorporated search data register and an output encoder. It starts a compare operation by loading an n-bit input search word into the search data register. The search data are then broadcast into the memory banks through n pairs of complementary search-lines SL and directly compared with every bit of the stored words using comparison circuits. Each stored word has a ML that is shared between its bits to convey the comparison result. Location of the matched word will be identified by an output encoder. During a pre-charge stage, the ML are held at ground voltage level while both SL and ~SL are at V_{DD}. During evaluation stage, complementary search data is broadcast to the SL and ~SL. When mismatch occurs in any CAM cell, transistor P_3 and P_4 will be turned on, charging up the ML to a higher voltage level. A sense amplifier (MLSA) is used to detect the voltage change on the ML and amplifies it to a full CMOS voltage output. If mismatch happens to none of the cells on a row, no charge up path will be formed and the voltage on the ML will remain unchanged, indicating a match.

In this paper the search speed boosting of CAM by introducing the parity bit is made. The rest of the paper is organized as Section I delay reduction of CAM with the introduction of parity bit, Section II performance analysis, Section III concludes the paper.

DELAY REDUCTION USING PARITY BIT

We introduce a versatile auxiliary bit to reduce the search delay there by speed boosting with a little area and power overhead. Before that the existing CAM architecture must be familiarized since our proposed method is similar to existing architecture but with different operating principle. The pre-computation CAM uses additional bits to filter some mismatched CAM words before the actual comparison.

These extra bits are derived from the data bits and are used as the first comparison stage. For example, number of "1" in the stored words are counted and kept in the Counting bits segment. When a search operation starts, number of "1"s in the search word is counted and stored to the segment on the left of Fig below. These extra information are compared first and only those that have the same number of "1"s (e.g., the second and the fourth) are turned on in the second sensing stage for further comparison. This scheme reduces a significant amount of power required for data comparison, statistically.

The main design idea is to use additional silicon area and search delay to reduce energy consumption. The previously mentioned pre-computation and all other existing de-signs shares one similar property. The ML sense amplifier essentially has to distinguish between the matched ML and the 1-mismatchML. This makes CAM designs sooner or later face challenges since the driving strength of the single turned-on path is getting weaker after each process generation while the leakage is getting stronger. This problem is usually referred to as I_{on}/I_{off}. Thus, new auxiliary bit that can concurrently boost the sensing speed of the ML and at the same time improve the I_{on}/I_{off} of the CAM by two times. Figure. 2. Shows the Pre computational CAM design.

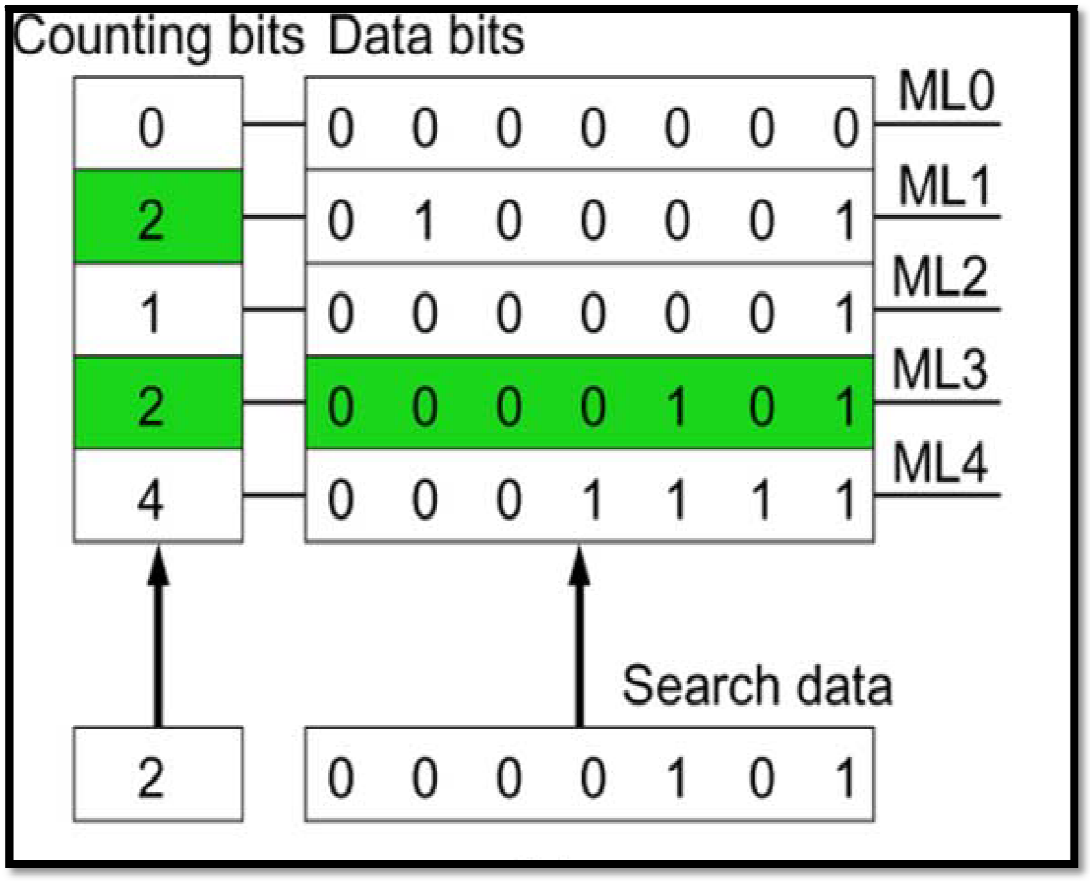

Figure. 2. Pre-Computational CAM Design

In the proposed parity bit based CAM design consisting of the original data segment and an extra one-bit segment, derived from the actual data bits. We only obtain the parity bit, i.e., odd or even number of "1"s. The obtained parity bit is placed directly to the corresponding word and ML. Thus the new architecture has the same interface as the conventional CAM with one extra bit. During the search operation, there is only one single stage as in conventional CAM. Hence, the use of this parity bits does not improve the power performance. However, this additional parity bit, in theory, reduces the sensing delay and boosts the driving strength of the 1-mismatch case (which is the worst case) by half, as discussed below. In the case of a matched in the data segment, the parity bits of the search and the stored word is the same, thus the overall word returns a match.

When 1 mismatch occurs in the data segment, numbers of "1"s in the stored and search word must be different by 1. As a result, the corresponding parity bits are different. Therefore now we have two mismatches (one from the parity bit and one from the data bits). If there are two mismatches in the data segment, the parity bits are the same and overall we have two mismatches. With more mismatches, we can ignore these cases as they are not crucial cases. The sense amplifier now only has to identify between the 2-mismatch cases and the matched cases. Since the driving capability of the 2-mismatch word is twice as strong as that of the 1-mismatch word, the proposed design greatly improves the search speed and Ion/Ioff ratio of the design. Figure.3. shows the speed boosting design using parity bit.

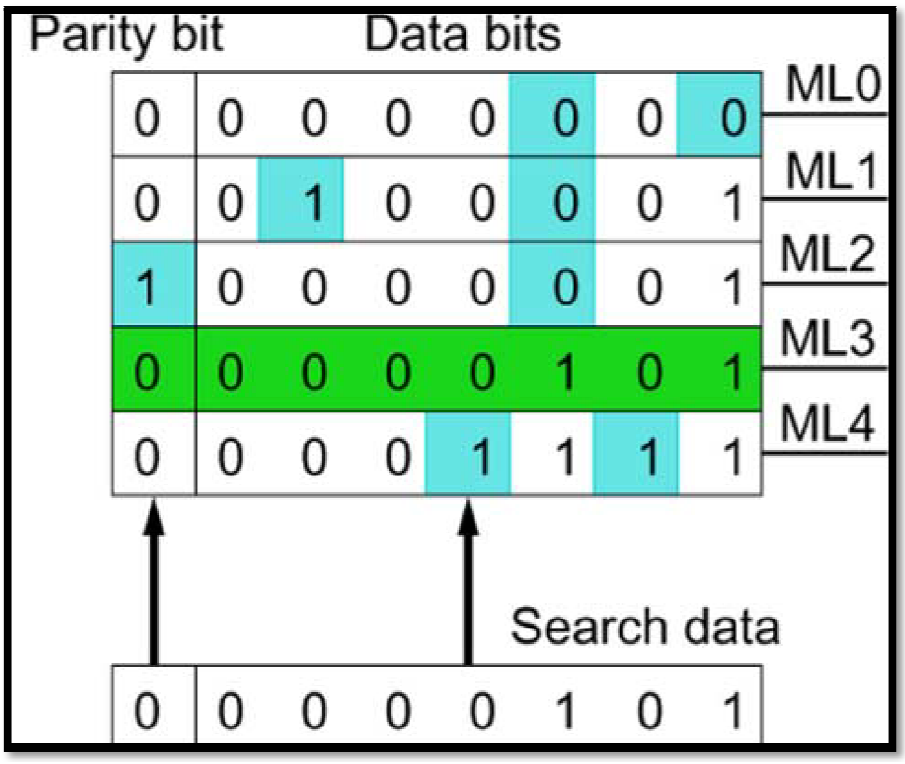

Figure. 3. Search Speed Boosting With a Parity Bit

PERFORMANCE ANALYSIS

The performance analysis of the proposed system is done by including the parity generator and there by replacing the 4bit counting bits data and replaced the parity bit along with the 8bit data input. After simulation it is obtained that with the inclusion of the parity bit the search speed delay is reduced to 2ns where as the original delay speed is about 6ns.This is evident in the simulation result that for the existing system the next address location of the word is fetched after 8 clock cycles where as with the inclusion of the parity bit instead of the counting bit it has been reduced to a single clock cycle. Hence it is observed that the search speed delay is reduced to 39%.Figure.4.shows the performance analysis graph of proposed and existing system.

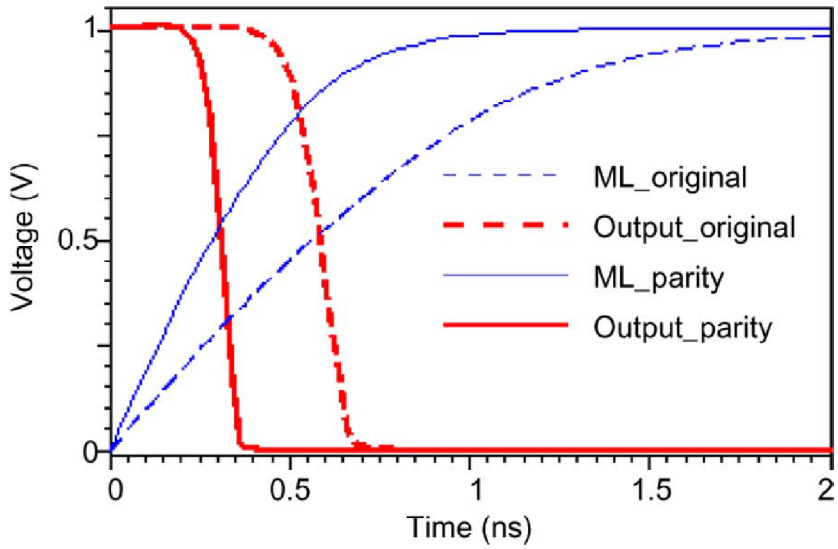

Figure.4. The Performance Analysis Graph Of Proposed And Existing System.

CONCLUSION

A high speed low power CAM with a parity bit was proposed. A CAM is a type of memory in which the contents are accessed by the words than memory locations. In the existing system design which is the pre-computation method we make use of the counting bit segment which is of 4 bit along with the input data and also with the words stored inside the cam memory this increases the number of steps in search operation by finding out the number of one's in the input bit and that stored in cam memory and this design methodology meets with I_{on}/I_{off} problem this altogether results in increase in search speed delay and additional silicon area consumption. In the proposed method we are introducing a parity bit instead of the counting bit which will reduce the search speed delay hence the output is fetched at an interval of one clock cycle. Since content addressable memory has wide application in the communication field the proposed design of cam can create revolutionary changes. This design helps to improve the search speed of cam and improve its efficiency.

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