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Technology Advances Beyond CMOS

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Abstract

As the dimensional scaling of CMOS eventually will approach fundamental limits, several new alternative information processing devices and microarchitectures are to be designed. The 'More Moore' domain is internationally defined as an attempt to further develop advanced CMOS technologies and reduce the associated cost per function. Almost 70% of the total semiconductor components market is directly impacted by advanced CMOS miniaturization achieved in the More Moore domain. The present paper introduces the recent advances and the perspectives in the beyond CMOS era development.

Key words: SOI (Silicon on Insulator), Dual gate FET, Strained Silicon, Carbon Nano Tubes, Graphene FETs.

Introduction

There are evolutionary and revolutionary advances that go beyond CMOS as in [1]. The advances that retain the standard CMOS paradigm are evolutionary and the advances using novel devices that break out of the standard CMOS paradigm are revolutionary. Silicon material reached its limits while shrinking device dimensions. Besides MOSFET, the alternative technologies to overcome the short channel effects and performance improvements are Silicon on Insulator (SOI), Dual gate FETs, Carbon Nanotubes (CNTs), etc.

Silicon on Insulator (SOI) Technology

Silicon on insulator (SOI) technology[2] refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing.This reduces parasitic device capacitance, thereby improves performance.The added advantage is the complete electrical isolation, so they are less

susceptible to radiation induced failure.Figure 1 gives the layer structure of an SOI.

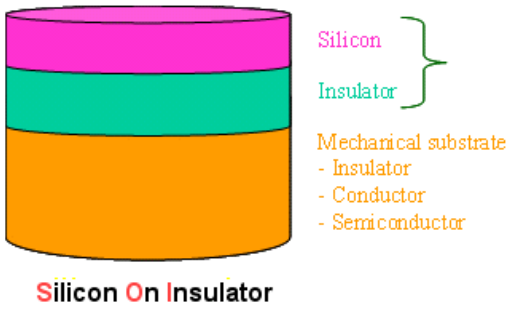

Fig 1 Layer structure of an SOI

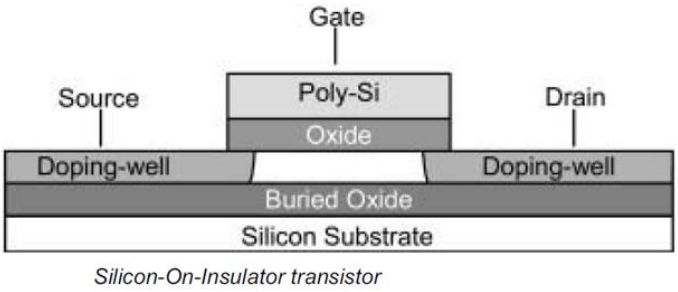

Fig 2 SOI Transistor

Dual Gate FETs

In dual gate FETs[4] there are two gates, front gate and back gate which controls the channel.Figure 3 gives the structure of a double gate MOSFET.

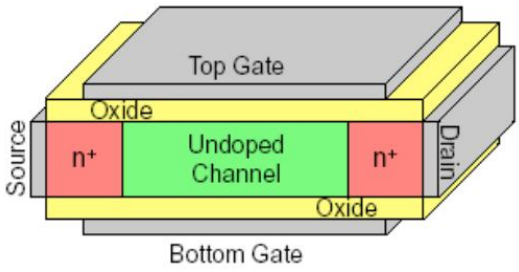

Fig 3 Dual Gate FET

The two gates shield the source region of the channel from the action of the drain. This increases the isolation between the source and drain. So short channel effects are reduced. The voltage applied on the gate terminals controls the electric field, determining the amount of current flow through the channel. The most common mode

of operation is to switch both gates simultaneously. Another mode is to switch only one gate and apply a bias to the second gate.

Several structures of dual gates are planar, non planar and FinFET [fig 4]. FinFET structure is so far the most promising.The major challenges are related to fabrication methods.

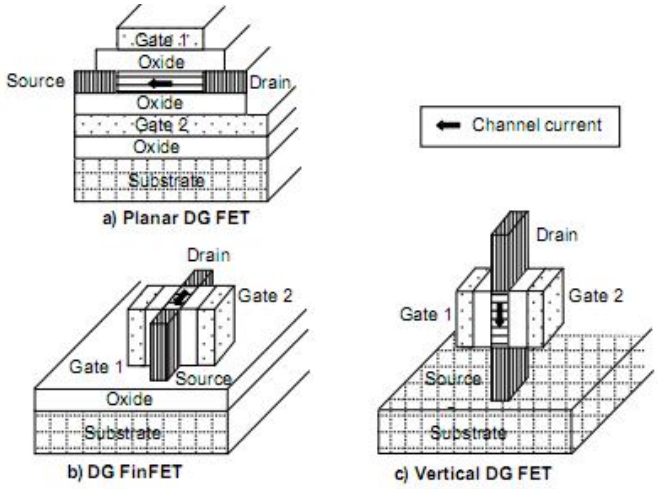

Fig 4 Dual Gate FET structures

FinFET is formed on a thin silicon on insulator (SOI) finger termed fin. On the top of the silicon fin nitride has been deposited on a thin pad oxide to protect the silicon fin during gate poly-SiGe etching. The gates are formed at the vertical sides of the fin using a thin gate oxide layer.

Strained Silicon

Strained silicon is a layer of silicon in which the silicon atoms are stretched beyond their normal interatomic distance as shown in figure 5.

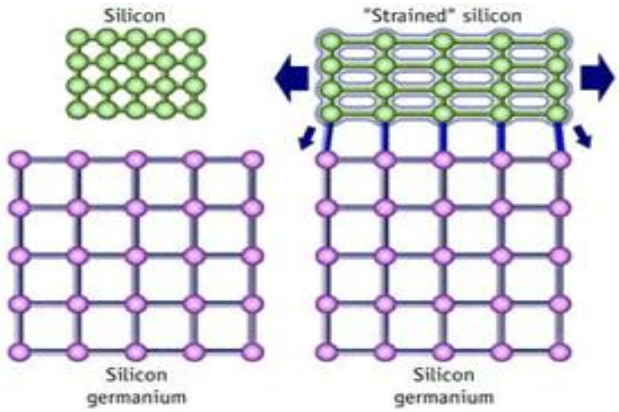

Fig 5 Strained Silicon

The Basic method is to change the lattice constant of material. Here Si and Si_xGe_{1-x} are the two dissimilar semiconducting materials used. SiGe has larger lattice constant than Si. So when one grows on top of another, either tensile force or compressive force is the result.The main advantage of this approach is that Strain in Silicon can increase mobility.

Carbon nano Tubes(CNT)

Carbon nanotubes are single sheets of graphite (called graphene) rolled into cylinders. The diameters of the tubes are typically of nanometer dimensions, while the lengths are typically micrometers. FETs based on CNTs are promising for RF circuits.

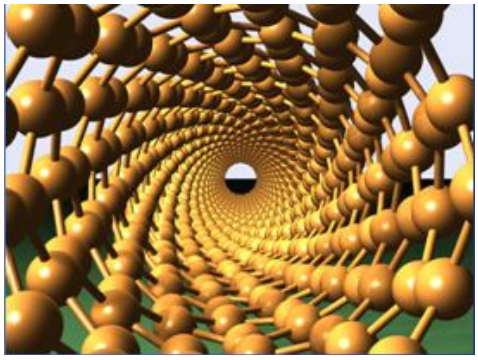

Fig 6 CNT

CNTs can be single walled carbon nanotubes (SWCNT) or multiwalled carbon nanotubes (MWCNT)[Fig 7].

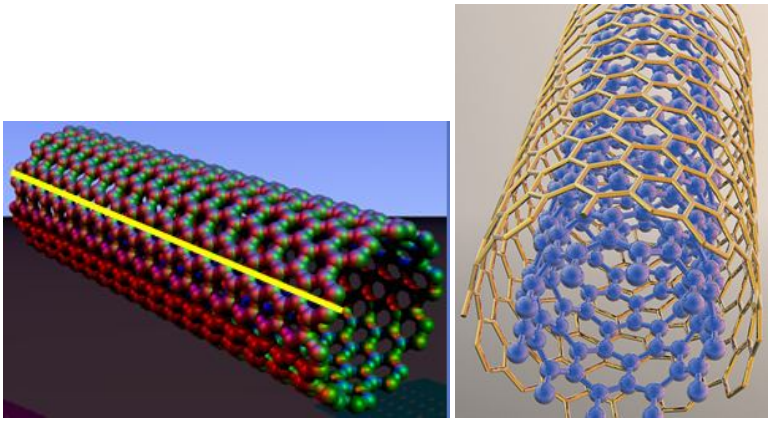

Fig7 Single walled CNT and Double Walled CNT

Since one CNT tube can carry only a current in the 10 - 30 μA range, arrays of hundreds of CNTs are required to obtain drain currents in the mA range [5], as

required for typical RF circuits. Unfortunately, the fabrication techniques known up to date do not allow growing semiconducting CNTs only.

Graphene FETs

Graphene has attracted attention for a range of electronic applications, such as displays, solar cells, and sensors owing to its exceptional electronic and optoelectronic properties. Graphene is a one-atom-thick planar sheet of carbon atoms that are densely packed in a honeycomb crystal lattice. In Graphene electrons / holes are confined to a plane of atomic thickness. This makes Graphene devices sensitive to the surrounding environment such as substrate and the dielectric media in contact with Graphene. Injected charge carriers are confined to a surface just one atomthick (~0.3nm).In principal, this allow graphene-based devices to push the limits of device scaling beyond those of silicon by enabling improved gate control and, therefore, reduced short channel effects in ultrashort channel devices. A schematic of graphene layer is shown in Fig 8. Work on graphene field effect transistors (FETs) [6], is proceeding at a rapid pace but is still at an early stage.

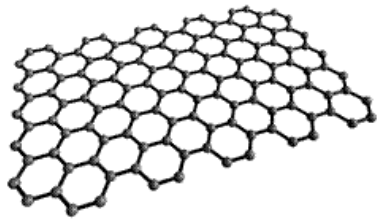

Fig 8 structure of graphene layer

Summary

Lot of researches are being done to design and implement reliable and durable high performance devices beyond CMOS.This paper gives a brief idea on some of the advances beyond CMOS.

References

[1] Kevin F Brennan, Introduction to Semiconductor Devices, Cambridge Publication

[2] F. Ellinger,M. Claus,M. Schröter and C. Carta, Review of Advanced and Beyond CMOS FET Technologies for Radio Frequency Circuit Design,Published in: Microwave & Optoelectronics Conference (IMOC), 2011 SBMO/IEEE MTT-S International.

[3] ITRS- International Technology roadmap for semiconductors, 2011.

[4] Bao Liu, Reconfigurable Double Gate Carbon Nanotube Field Effect Transistor Based Nanoelectronic Architecture, Published in Design Automation Conference, IEEE, 2009.
[5] M. Claus, M. Schröter, "Design study of CNT transistor layouts for analog circuits", Proc. NSTI Workshop on Compact Modeling, 2009, 3,pp. 566 – 569.
[6] Meric, I. Dean, Cory ; Young, A. ; Hone, J. ; Kim, Philip ; Shepard, Kenneth L. , Graphene field-effect transistors based on boron nitride gate dielectrics, Published in Electron Devices Meeting (IEDM), 2010 IEEE International.