International Journal of Electronics and Communication Engineering.
ISSN 0974-2166 Volume 6, Number 1 (2013), pp. 81-92

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Low Power Consumption Differential Ring Oscillator

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Abstract

The design of Oscillator is need of to days circuits, The PLL uses this oscillator for different devices. The use of ring oscillator gives benefit in term of size and wide tuning range. We can use LC oscillators for low noise, but on the cost of area needed. To improve performance of circuit we uses differential delay cell. This work is based on review of different VCO. The ring oscillator with differential stages are the one which fulfil the parameter which we are analysed.

Keywords: CMOS, low power, ring oscillator, differential delay cell.

Introduction

The design of clock circuit for microprocessor to carrier synthesis in wireless communication needed different Oscillator circuits. The PLL used in wireless devices, PLL needed Oscillator. There is different oscillator waveform oscillator and resonant oscillator. The wave form oscillator include Ring oscillator and relaxation oscillator, similarly resonsnt oscillator having LC oscillator and Crystal oscillator. LC oscillator has low phase noise but low frequency swing. They are used in wireless application. On the other hand the ring oscillator is widely used in integrated circuit. Ring oscillators are being used by semiconductor foundries to monitor power dissipation, delay, and jitter of fabricated CMOS inverters. On the basis of result of measured frequency pattern we accept or reject the IC. Ring oscillator also occupies less chip area as they do not have inductor as compared to LC tank oscillator. As the LC oscillators are less prone to noise. The main objective of paper to review the ring oscillator on the basis of different parameter.

Oscillator

Oscillator are integral part of many electronic systems application rang from clock generation in microprocessor to carrier synthesis in cellular telephones requiring vastly different oscillator topologies and performance parameter.[4] Recently the explosive growth in wireless communication and the advances in complementary metal oxide semiconductor(CMOS) technology made it possible to implement high frequency oscillator with CMOS technology.[MR20768] The oscillator are required to be tunable over a relatively wide frequency rang. The tenability is usually obtained by variable voltage and hence comes the name Voltage Controlled Oscillator (VCO). VCOs are key component in frequency synthesizer for Radio Frequency (RF) wireless application. [5] Voltage *Controlled Oscillators (VCOs)* constitute a critical component in many RF transceivers and are commonly associated with signal processing tasks like frequency Selection and signal generation. RF transceivers of today require programmable carrier frequencies, and rely on phase locked loops (PLLs) to accomplish the same. These PLLs embed a less accurate RF oscillator in a feedback loop whose frequency can be controlled with a control signal. [6]

Types of VCO

The Analog Group, of the UW ASIC Group, has decided to concurrently design two different VCO (Voltage Controlled Oscillator) topologies. This introduction provides some of the reasoning for why the Analog Group has chosen to design VCOs that have the ring oscillator and the LC tank topology. There are two types of VCOs that one may choose to design:

1) Waveform oscillators
2) Resonant oscillators.

Waveform oscillators:

1) Ring oscillator topology
2) Relaxation oscillator (which has poor phase noise performance).

Resonant oscillators:

1) LC tank oscillator topology
2) Crystal oscillator (which is neither integrated nor tunable).

Ring Oscillator

Single ended ring VCO

The ring oscillator is basically a closed loop comprised of an odd number of identical inverters, which form an unstable negative feedback circuit. The period of oscillation is twice the sum of gate delays in ring comprises inverters. A voltage control ring oscillator CMOS inverter first used for clock recovery in an Ethernet controller [1]. Since then ring oscillator widely used in wireless devices. A simple ring oscillator is just a inverter chain in odd number, to make negative feedback we use a buffer to

make number of stages even. So that the feedback help in oscillation. The figure 1[2] Show single end VCO.

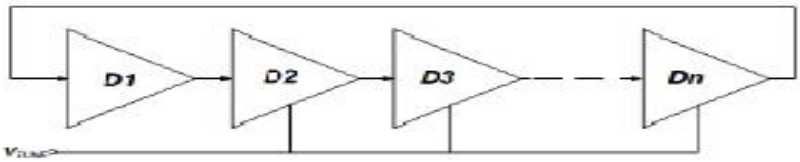

Figure 1: Single end ring VCO.

Differential loop ring oscillator

The differential oscillator has output to reject common-mode noise, power supply noise. The CMOS used in differential form. Figure 2[2] show the ring oscillator with 3 stage ring oscillator with differential cell. A simple ring oscillator is just differential inverter chain in odd number, to make negative feedback we use a buffer to make number of stages even. So that the feedback help in oscillation

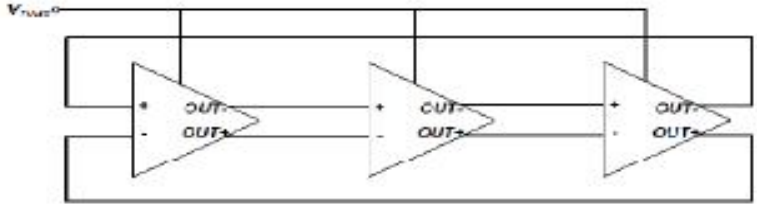

Figure 2.3: Stage differential ring oscillator.

The differential ring oscillator is widely used, since it has a differential output to reject common-mode noise, power supply noise and so on. In this VCO a differential type is used. As from figure2, if it has N stage than N stage ring oscillator realized using differential cells (which have complementary output).A source coupled pair (SCL) inverter will be a typical implementation. Assume that at time t0 the output of stage 1 changes to logic 1.when this logic 1 propagates to the end, it creates a logic 1 at the Nth stage, which, when feedback to the input of the first stage, creates a logic 0 in the first stage output. When this logic 0 is propagating through the chain, it toggles the output of stage 1 trigger next stage. It takes two passes through the chain to complete a period. Denoting tp as the propagation delay through each stage, then period T=2Ntp.for a single ended output cell, N has to be odd, but for a differential cell N can be odd/even, to start an oscillation.

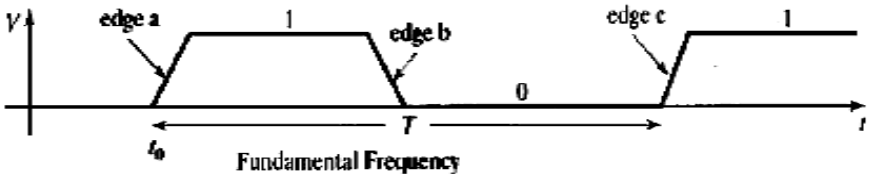

Figure 3: Fundamental Frequency.

Phase noise

The ideal VCO will provide only one pure sinusoidal wave, but in reality, the periodic signal from the VCO would contain other frequency signals that can be random or not. As figure: 3 shows [2]

LC Tank VCO Basic

A general LC-VCO can be shown as in Figure 1. The inductance *L* and the capacitance *C* consist of a parallel resonance tank. *RL* and *RC* are the parasitic resistances of *L* and *C*, respectively. In order to compensate the losses coming from *RL* and *RC*, active components like CMOS transistors are used to realize a negative resistance $-R$. According to [5], the loss in the tank can be expressed as

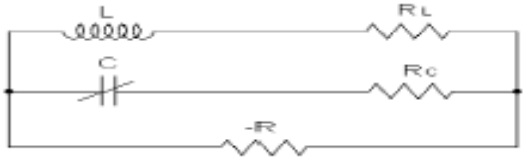

Figure 3. A basic LC VCO

$$Ploss = 4\pi^2 RC^2 f_0{}^2 Vpeak^2 = \frac{R}{4\pi^2 L^2 f_0{}^2} Vpeak^2 \quad (4)$$

Where *R* represents the combined losses of the inductance and the capacitance, and V_{peak} is the peak voltage amplitude across the capacitance. It can be observed from (1) that the power loss decreases linearly with the series resistance in the resonance tank, and it also decreases quadratically with an increase of the tank inductance.

In order for the resonance tank to resonate without any loss coming from parasitic, the parasitic resistance and capacitance coming from both the inductor and resistor need to be compensated. As for the compensation for parasitic resistance, a negative resistance, -R is formed in the tank in order to cancel out both of the parasitic resistances. However, in a real form, negative resistance does not exist. a negative resistance is formed by cross-coupling transistors that are connected to the resonant tank.

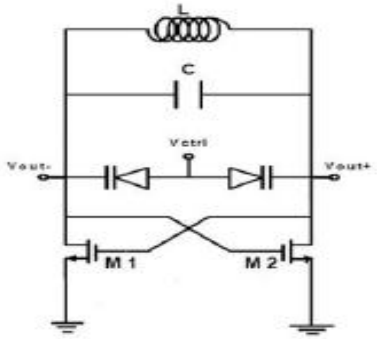

Figure4: A Cross Coupled Oscillator.

By cross-connecting the output to the input of the oscillator, negative resistance that has the same conductance as the transistor's transconductance (gm) is created. The phase noise of a LC-VCO is inversely proportional to the Q^2 [7], where Q is the equivalent quality factor of the LC-tank. Since the quality factor of varactors are more than inductors, thus the quality factor of inductor plays dominant role in the Q of tank. The CMOS inductors in RF circuits suffer from low quality factor. So, if one can increase the Q of the LC-tank, the phase noise will be improved. For this goal, we have used added negative transconductance technique in the LC-VCO. The quality factor of a LC-tank can be expressed as bellow:

$$Q= 1/G_{tot}\sqrt{(C/L)} \quad (5)$$

Where G_{tot} is the transconductance of the LC-tank that can be confined with quality factor of the inductor. We can express G_{tot} as follow:

$$G_{tot}= G_P-G_N \quad (6)$$

Where G_N is the added negative conductance to the circuit that can decrease G_{tot} and therefore increase Q of the LC-tank. [8]

A typical LC tank VCO consists of LC resonator tank to provide oscillation. This oscillation phenomenon employs the concept of "negative resistance". The resonator can be equivalent to a parallel *RLC* tank circuit, whose *Rp* (parallel resistance) captures the energy loss inevitable in any practical system. If a resistor equal to *-Rp* is placed in parallel with *Rp* , as shown in Figure 1, since *Rp* // (*-Rp*) = ∞, the tank oscillates at ω_0 indefinitely. Thus, if a one-port circuit exhibiting a negative resistance is placed in parallel with a tank, the combination may oscillate. This topology is called as negative resistance model. [8]

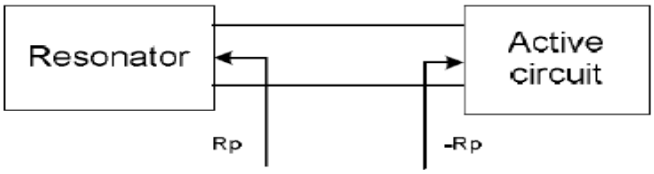

Figure5: A simple negative gm oscillator block diagram.

VCO Specification

Ideally a given VCO topology would be able to meet all of the specifications listed below:

1) Phase noise
2) Tuning range
3) Power Consumption
4) FOM

Phase noise

Phase noise is generally characterized in the frequency domain. The output of an ideal oscillator may be expressed as:

$$V_{out}(t) = V_0 \cos[\omega_0 t + \phi_0] \quad (6)$$

Where the amplitude, V_o, the frequency, ω_0, and phase reference, φ_o, are all constants. The spectrum of an ideal oscillator consists of an impulse at ω_0. However, when using a real oscillator, the amplitude and the phase are affected by noise and are time-variant, so the output is now:

$$V_{out}(t) = A(t)\cos[w_o t + \emptyset(t)] \quad (7)$$

Where $\varphi(t)$ is called the excess phase of the output. The spectrum of this signal has sidebands close to the frequency of oscillation f_0. These instabilities in amplitude and phase can be characterized quantifying the single sideband noise spectral density around the carrier ω_0 [9]. It has units of decibels below the carrier per hertz (dBc/Hz) and is defined as:

$$\mathcal{L}_{total}(\Delta w) = 10 \log \frac{Psideband(w_0 + \Delta w, 1Hz)}{P_{carrier}} \quad (8)$$

The spectrum of an ideal oscillator consists of an impulse at ω_0, as shown in Figure 6 (a). The output spectrum has power around ω_0 if the waveform, *f*, is not sinusoidal, as shown in Figure 6 (b).

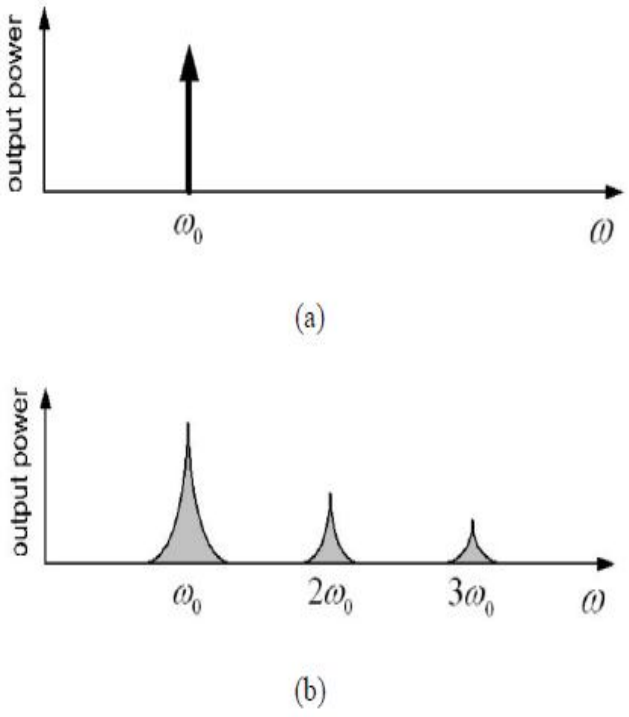

Figure 6: Spectrum of (a) an ideal oscillator and (b) a real oscillator.

Tunning Range

Most wireless applications require a tunable oscillator, which means its output frequency is a function of a control input, usually a voltage. An ideal VCO is a circuit, whose output frequency is a linear function of its control voltage (V_{con}), as shown in Figure 2.16,

$$f_{out} = f_o + K_{VCO} \cdot V_{con} \tag{9}$$

Where, f0 is the oscillation frequency at Vcon = 0 and KVCO represent the gain or sensitivity of the circuit. The achievable range, f2–f1, is called the frequency tuning range.

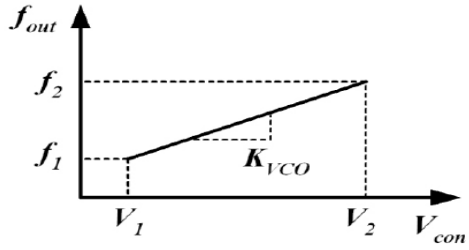

Figure 7: Definition of KVCO.

Frequency tuning is required not only to cover the whole application bandwidth but also to compensate for variations of the centre frequency of the VCO that are caused by the process and by temperature. The oscillation frequency of an LC-tank VCO is approximately equal to $f(LC)_{osc}$,= $1/(2\pi \sqrt{LC})$ so that only the inductor and capacitor values can be varied to tune the oscillation frequency.

Power Consumption

Mobile devices are required to have long standby times, indicating a need for low power consumption. In a VCO design, it is difficult to have low phase noise with low power consumption simultaneously because the tank voltage amplitude is proportional to the current flowing. Therefore, there is a trade-off between phase noise and power consumption. It is presented in the Leeson's phase noise model.

The voltage amplitude of the tank for the CMOS cross-coupled differential topology can be expressed by assuming that the differential stage switched from one side to the other. As the tank voltage changes, the direction of the current flow through the tank reverses. The differential pair can be modelled as a current source switching between I_{total} and $-I_{total}$ in parallel with an RLC tank. R_{eq} is the equivalent parallel resistance of the tank. The tank amplitude can be approximated as

$$V \approx I_{total} \cdot R_{eq} \tag{10}$$

This is referred to as the current-limited operation because tank amplitude mainly depends on the total current flowing and the tank's equivalent resistance. However, (3.14) becomes invalid when the tank amplitude becomes the supply voltage through

an increase of Itotal. This operation is called the voltage-limited operation [18]. With currentlimited operation, as the current increases (consuming more power), the phase noise lowers because the tank amplitude is increasing simultaneously.

Figure of Merit

To evaluate a designed VCO compared with other VCOs in terms of performance, one of the general Figure-Of-Merit (FOM) formulas is expressed as

$$FOM = L(\Delta w) - 20.\log\left[\left(\frac{w_o}{\Delta w}\right)\right] + 10.\log\left(\frac{P_{diss}}{1mW}\right) \quad (11)$$

Equation 11 includes phase noise, L(Δω) at an offset frequency of Δω, oscillation frequency, ω_0, and power consumption of the core circuit, P_{diss}.

Proposed Ring Oscillator Design

The proposed ring oscillator for VCO is differential Ring oscillator. We want to improve noise performance of the ring oscillator, so differential ring VCO is used to reduce noise.

Differential Delay Cell

A basic differential delay cell is shown in Figure 3[3]. It is used to reject the common mode and power supply noise.

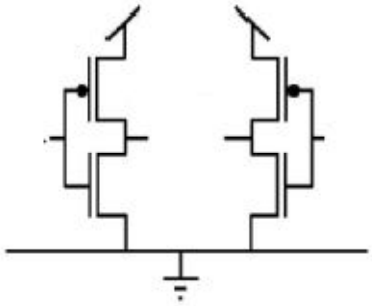

Figure 3: Basic Delay Cell.

A basic differential ring oscillator has two differential inputs as compared to one in case of basic ring oscillator. A buffer stage is added to make the output stable, so the there are total 4 stage of figure. 4[3]

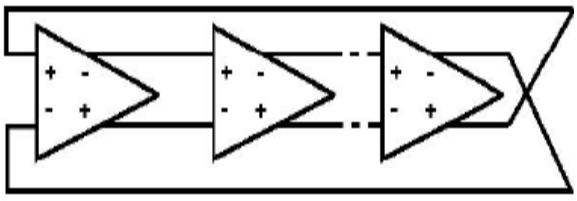

Figure 4: Basic Differential Ring Oscillator

Ring Oscillator Design

We are making the circuit with two CMOS inverter stage and one CMOS Nand gate. As Shown if in figure[5][3]. The Nand gate with same input behave as a inverter and make 3 stage circuit of ring oscillator. Each inverter adds some delay known as 'inverter pair delay'. The inverter pair delay is given by sum of rise time and fall time. The frequency of oscillation is given by as:

Fosc= 1/ N(Trise + TFall)

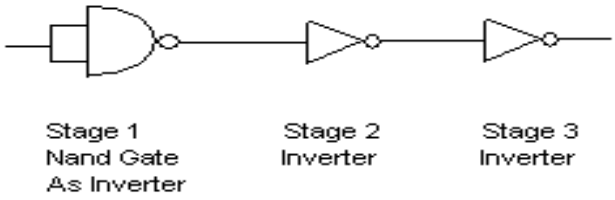

Figure 5: Schematic of Proposed Design.

Where τrise and τfall are the rise and fall time of a individual delay cell or stage. For a good VCO rise time and fall time should be equal. Thus taking τrise = τfall = τ. As a three stage ring oscillator is presented in this paper so by taking the value N=3, the frequency of oscillation is given as:

For the inverter shown in Figure 5, the (W/L) ratios of the transistors (nMOS and pMOS) are given as:

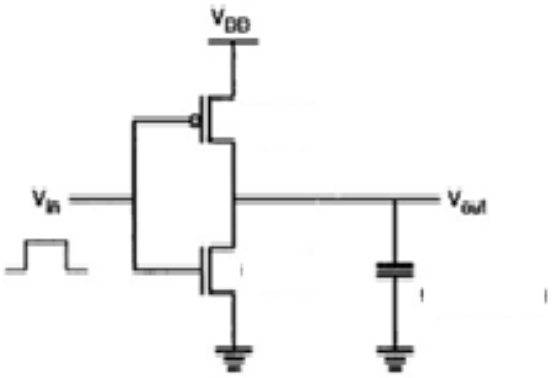

Figure 5: CMOS Inverter.

There are many features that differentiate the delay cell used in ring oscillator. The most important is slew time that determines the overall phase noise performance. There are three categories of delay cell. [5]First is fast slewing saturated delay cell. This delay cell has fast rise and fall time. It also performs full switching and therefore belongs to the saturated class of delay cell. The second type of delay cell is a slow slewing saturated delay cell. Here the inverter consists of a source of a source coupled pair (SCP) and hence this is a current based inverter. It is called slow slewing because

it has a longer gate delay. The third type of delay cell is non saturated delay cell. This is also a voltage inverter based delay cell. In this delay cell some transistors are never on/off as a result output waveform never reach Vdd or ground, which is why this type of delay cell is called non saturated.
A slow slewing saturated delay cell is used which is shown in figure 7[2]

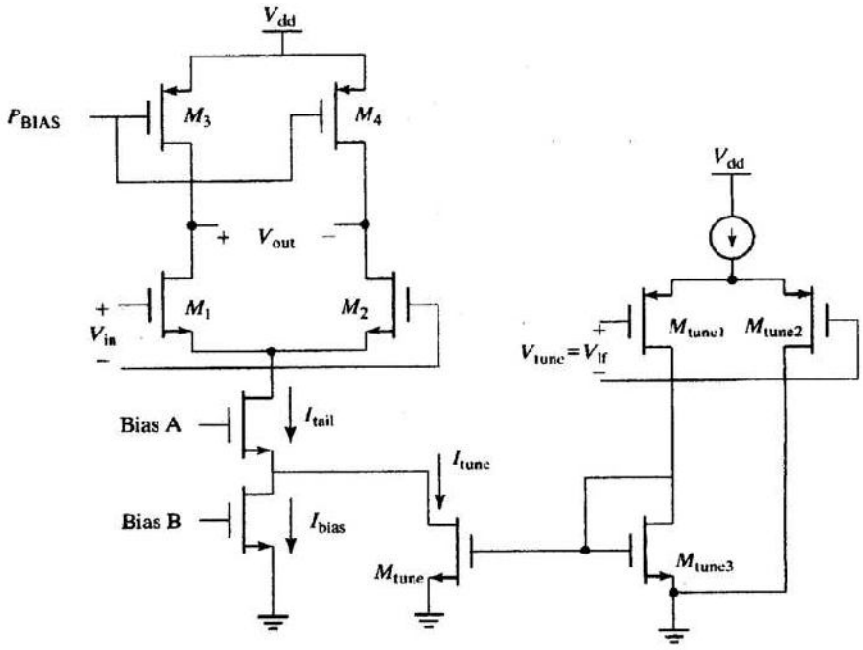

Figure 7: Slow Slewing Saturated delay cell.

Comparison and Discussion

From this comparison table we seen that the ring oscillator[3] are better than the LC[12], colpitts[10] and Hartley oscillator[11], in tuning range and power consumption. This is due to new structure of it with odd stages by removing buffer stage.

Table I: Comparison of parameter.

Reference	**Type**	**Process Technology**	**Power**	**Tuning raange**
Ref.10	**Colpitts VCO**	**0.18CMOS**	**6.4**	**4.9-5.46**
Ref.11	Hartley VCO	0.18CMOS	6.75	4.02-4.5
Ref.12	LC VCO	0.18CMOS	13.7	4.55-5.45
Ref.13	Ring VCO	0.18CMOS	27	5.16-5.93
Ref.3	Ring VCO	0.18CMOS	.621	3.125-5.26

Conclusion

The Ring oscillator can be used in place of LC oscillator, but it causes noise in circuit. So we can use differential oscillator in place of inverter chain. We are using 3 stage design of differential ring oscillator to improve power consumption.

References

[1] A. Bell and G. Borriello, "A single chip nMOS Ethernet controller," IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers, 1983, pp. 70–71.

[2] Mrs. Devendra Rani "A Voltage Controlled Oscillator using Ring Structure in CMOS Technology" International Journal of Electronics and Computer Science Engineering ISSN- 2277-1956.

[3] Ashish Raman, Jaya Nidhi Vashishtha1 and R K sarin "A RF Low Power 0.18-µm based CMOS Differential Ring Oscillator" World Congress on Engineering 2012 Vol II WCE 2012, July 4 - 6, 2012, London, U.K.

[4] Behzad Razavi "Design of Analog CMOS Integrated Circuit" Tata McGraw Hill pvt ltd, Edition 2002, Eighteenth reprint 2010.

[5] Yua Zing Yao, "comparative study of low phase noise voltage controlled oscillator (VCOs) in CMOS Technology" M. Sc., Concordia University, Montreal, Quebec, Canada, Jan.2006.

[6] Chetan Shambhulinga Salimath, "DESIGN OF CMOS LC VOLTAGE CONTROLLED OSCILLATORS" M. Sc., Visveswariah Technological University, India, India, December 2006.

[7] Mohammad Niaboli-Guilani" A Low Power Low Phase CMOS Voltage Controlled Oscillator" 17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2010.

[8] M.A. Nandanwar, M.A.Gaikwad, D.Dandekar, "Low Power Low Phase Noise CMOS LC VCO–A Review", International Journal of Applied Information Systems (IJAI*S)*, Vol. 3, pp. 37–41, July 2012.

[9] *Jie Long, Jo Yi Foo, Robert J. Weber,* "A *2.4 GHz Low- Power Low-Phase-Noise CMOS LC VCO*,"VLSI,IEEE computer Society Annual Symposium on (2004), pp.213- 214.

[10] J.-A. Hou and Y.-H.Wang, "A 5 GHz differential Colpitts CMOS VCO using the bottom PMOS cross couple current source," IEEE Microwave and Wireless Components Letters Vol. 19, No. 6, PP. 401–403, June 2009.

[11] S.-H. Lee, Y.-H. Chuang, S.-L. Jang, and C.-C. Chen, "Low phase noise IEEE Microwave and Wireless Components Letters Vol. 17, No. 2, PP. 145–147, February 2007.

[12] C. Samori, S. Levantion, and V. Boccuzzi, "A -94 dBc/Hz @100 kHz fully-integrated, 5-GHz CMOS VCO with 18% tuning range for bluetooth

applications," in Proceedings IEEE Custom Integrated Circuits Conference, 2001, PP. 201–204.

[13] Y. A. Eken and J. P. Uyemura, "A 5.9-GHz voltage-controlled ring oscillator in 0.18-µm CMOS," IEEE J. Solid-State Circuits, vol.39, No. 1, pp. 230-233, January 2004.

[14] Sheng Lyang Jang, Chih Chieh Shih, Cheng Chen Liu and Miin Horng Juang, "A 0.18µm CMOS Quadrature VCO Using the Quadrature Push-Push Technique", IEEE Microwave and Wireless Components Letters, Vol. 20 No. 6, June 2010.

[15] S. Loo, B. G. Colpitts, and D. M. Luke, "Fully-integrated bipolar differential VCOs at 2.95 and 5.7GHz," froc. q/ 2000 lEEE Canadian

[16] Conference on Electrical and Computer Engineering, vol. 2, pp. 797-801.

[17] J. Plouchart, H. Ainspan, M. Soyuer, and A. Ruehli, "A fully-monolithic SiGe differential Voltage-Controlled Oscillator for 5 GHz wireless applications," Proc. of2000 IEEE RFIC Symposium, pp.57-60.

[18] H. R. Rategh, H. Samavati, and T. H. Lee, "A CMOS frequency synthesizer with an injection locked frequency divider for a 5-GHz Wireless LAN receiver," IEEE J. of Solid-State Circuits, vol. 35, no. 5, pp. 780-787, May 2000

[19] G. Gtau, U. Langman, W. Winkler, D. Knoll, J. Osten, and K. Pressel, "A current-folded up-conversion mixer and VCO with ccnter-tapped inductor in a SiGe-HBT technology for 5-GHz Wireless LAN applications," lEEE J. of Solid-State Circuits. vol. 35, no. 9, pp. 1345-1351, Sep. 2000.