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A Low complexity solution to the implementation of linear periodically time varying filters-FPGA implementation

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ABSTRACT

This paper presents an area efficient architecture for a linear periodically time varying (LPTV) filter. It is developed from the output switching representation of LPTV filter. In this representation, an *N*-tap,*M* Period LPTV filter can be realized by *M* linear time invariant (LTI) filters of *N* taps each connected in parallel with an *M* periodic switch at the output. We devloped an area efficient architecture for LPTV filter from a single *N* tap LTI filter. We achieve this by distributing the coefficient memory. The proposed architecture utilizes *N* coefficient multipliers, whereas the conventional output switching realization needs *NM* multipliers. The proposed architecture is simulated, synthesized and implemented on Virtex FPGA.

Keywords: LPTV, Output switching representation, FPGA

I. INTRODUCTION

Linear periodically time varying (LPTV) systems have numerous applications in variousfields such as signal processing, communications and control systems. Some of the significant applications include spread spectrum [1], trans multiplexing [2], blind channel estimation [3], spectral scrambling [4], temporal scrambling [5], digital watermarking of natural images [6], sample data systems and multi-rate filter banks.

LPTV systems are generalizations of linear time invariant (LTI) systems.For an LPTV system with period *M*, when the input is delayed by *M* samples, so will be the shift in the output. Hence an LTI system can be viewed as an LPTV system with

period '1' [7]. LPTV systems can be realized using various structures. In [8] various structures for an LPTV filter and their interrelationships are discussed. An important representation of LPTV filters is using periodic switching and LTI filters. The LPTV system operation is more illustrative from this representation. Interested reader may refer [9] for further analysis of this representation. It was observed in the past works that LPTV filters come naturally in the multirate filter design.

Most of the previousworks concentrated on VLSI implementation of LTI filters [11-13]. In this paper we consider the VLSI implementation of LPTV filters, using switching representation. We discuss the VLSI implementation starting from LTI filters and develop a solution for efficient LPTV filter implementation. Because of stability and linear phase response, we prefer the FIR LTI filters.

Since the coefficient multipliers in FIR filter realization consume larger power and area, the main focus is on the multiplier design. In [11], [12] efficient design of multipliers to reduce area complexity and power consumption was discussed. In [13], polyphase half-band FIR filters and band pass filters IIR filters are realized. VLSI implementation of a 64×1 FIR decimator was proposed in [14].

In literature no details of the VLSI implementation of LPTV filter is available.

Hence we propose an area efficient architecture for output switching representation of LPTV filter, which has the complexity of LTI filter.

The organization of the paper is as follows. Section II discuss about basics of LPTV filter. Section III explains the proposed LPTV filter design. Simulation and synthesis results are presented in section IV and conclusion is presented in section V.

II. BASICS OF LPTV SYSTEMS/FILTERS

Any linear system can be called as an LTI system, when the output of the system is delayed by the same number of samples so as the input. A generalization of LTI system is LPTV system. For an LPTV system of period *M*, when the input is shiftedby *M* samples, the output also undergoes corresponding shift of *M* samples.

From the definition of LPTV filter, we know that the coefficients of LPTV filter vary periodically. Hence, we can express the output in terms of input as

$$y(n) = \sum_{k=-\infty}^{\infty} g_l(k)x(n-k), \tag{2}$$

where $l = n \bmod M$, by generalizing the convolution sum.
If we assume,

$$y_l(n) = g_l(n) * x(n), \tag{3}$$
$$y(n) = y_l(n), \tag{4}$$

when $l = n \bmod M$

From (3) and (4), we can conclude that among the outputs $y_l(n)$ of the filters $g_l(n)$, we are picking the output based on n value from the relation $l = n \bmod M$.

Thus we can obtain the structure as shown in Figure1. Obtaining one output among *M* can be realized as switching operation.

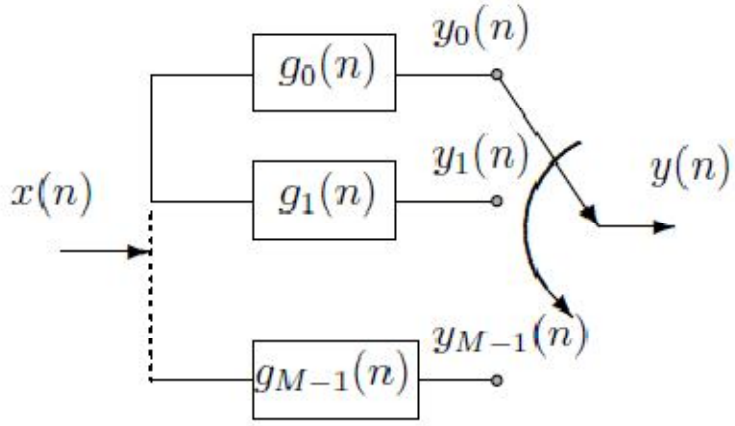

Figure. 1: LPTV filter in Output Switching Representation

The hardware implementation of LPTV filter shown in Figure. 1 consists of *M* LTI filters. If we consider an *N*-tap LPTV filter, then each LTI filter in Figure1 has *N* taps. The number of multipliers required to implement each LTI is *N*. Hence the total number of multipliers required to realize the LPTV filter is *MN*. The direct form structure of one such LTI is shown in

Figure 2.Clearly, *N* multiplications are required to compute the output of each of the *M* filters.

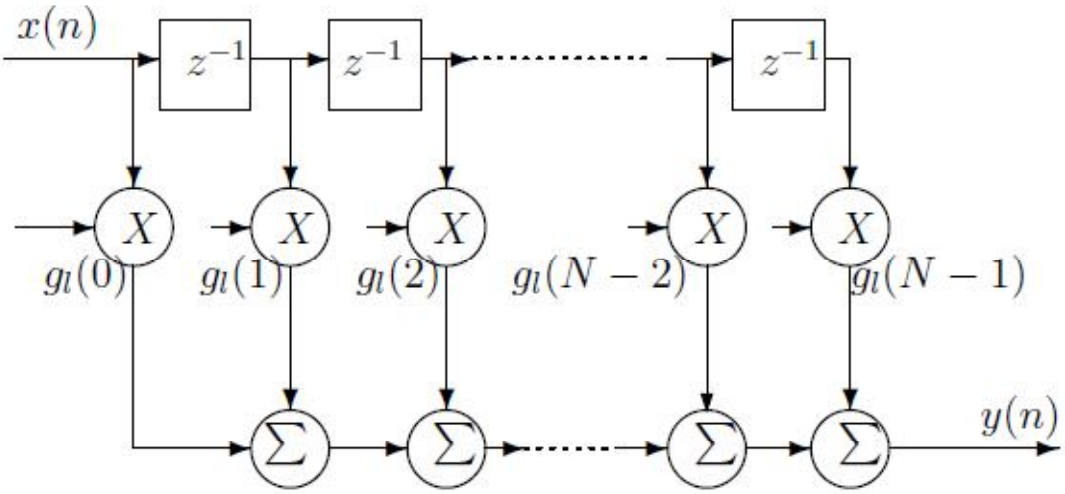

Figure. 2: Structure of LTI in output switching representation of LPTV filter

However, the output of only one filter is picked up at a time and the outputs of all the remaining (*M*-1) filters' computations are wasted. So the computations performed

for obtaining all these outputs go in vain. The multipliers utilized for these computations are unnecessary.

To overcome this problem, we realize the LPTV filter with a different architecture, where in a single LTI filter architecture performs the LPTV operation by distributing the coefficient memory.

III. PROPOSED LPTV ARCHITECTURE

We propose an LPTV filter architecture whose complexity is close to that of an LTI filter realization. Instead of storing all the coefficients $g_l(.)$ in a single memory, we distribute and store them as coefficient banks in SRAM look up tables (LUTs). There are N banks and each bank consists of M coefficients from $g_0(.)$ to $g_{M-1}(.)$. The address lines of the coefficient banks are enabled by each clock cycle n in such a way that $g_l(q)$ is selected from q-th coefficient bank when $l=n \bmod M$. For example consider M=4 and clock cycle n=20, the output of first coefficient bank consisting of $g_0(0)$,$g_1(0)$,$g_2(0)$……,$g_{M-1}(0)$ will be $g_0(0)$.

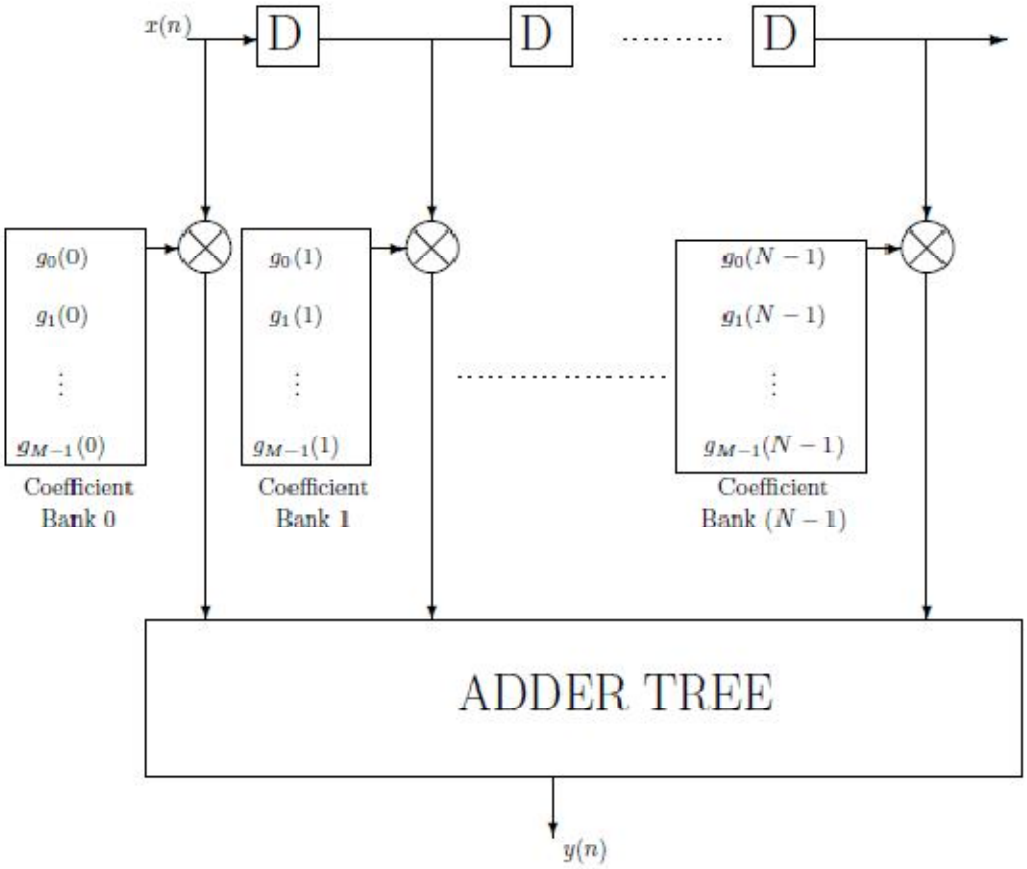

Figure. 3: Proposed LPTV filter architecture

The proposed architecture is shown in Figure. 3. It consists of *N* multipliers and *N* coefficient banks. Each coefficient bank stores *M* coefficients. Appropriate coefficients are accessed from the bank and are given to the corresponding multiplier. The outputs of all the multipliers are given to the adder tree to produce the convolution sum.

The proposed realization of LPTV filter requires *N* multipliers where as realization of LPTV filter in conventional output switching representation needs *MN* multipliers. Since the number of multipliers is reduced from *MN* to *N*, the proposed architecture reduces the area complexity as well as power consumption.

By comparing Figure 2 and Figure 3, it is easy to note that LPTV filter is realized just like LTI filters with distributed coefficient memory.

IV. SIMULATION AND SYNTHESIS RESULTS

To support the theory developed so far, simulations are carried out using VHDL. We synthesized and implemented the original switching representation and the proposed structure on Virtex FPGA. We considered a 32- tap, 4 period, and LPTV FIR filter . It can be realized as a single 32 tap LTI filter with the architecture shown in Figure3. The direct implementation of LPTV filter using output switching representation in Figure1 and the proposed LPTV filter in Figure 2 are simulated using VHDL.

The simulation waveforms of the original structure and the proposed structure are shown in Figure 4(a) and Figure4(b) respectively. The sampling frequency selected for simulating the designs is 10 MHz. If we observe the output of the first design, for the given input *x,* all the four filters are operating and giving the outputs *y0* to *y3* in each and every clock cycle. They are assigned to the output *y* in a cyclic order. Hence at any time, only one output is utilized and the remaining three filters result in wasted computations. Where as in the proposed design only the desired output is obtained from the LTI by accessing the coefficient banks accurately. From Figures 4(a) and 4(b), we can conclude that the final output *y* is same for both the structures.

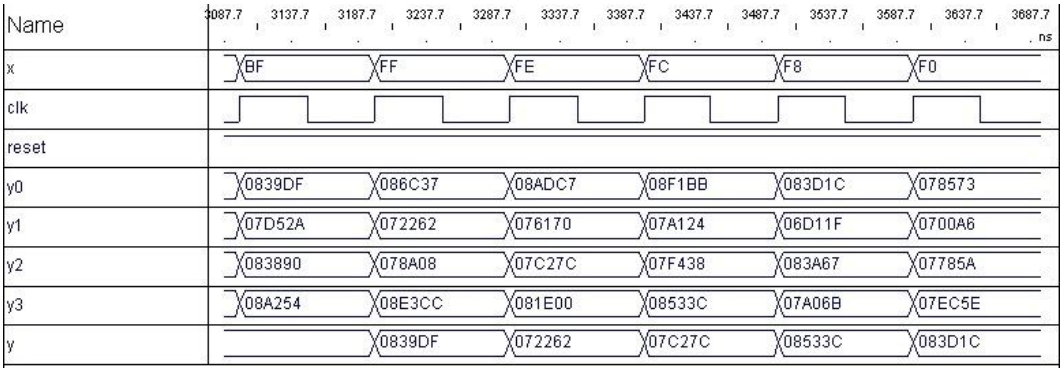

Figure 4(a): Simulation Results of Conventional LPTV Filter

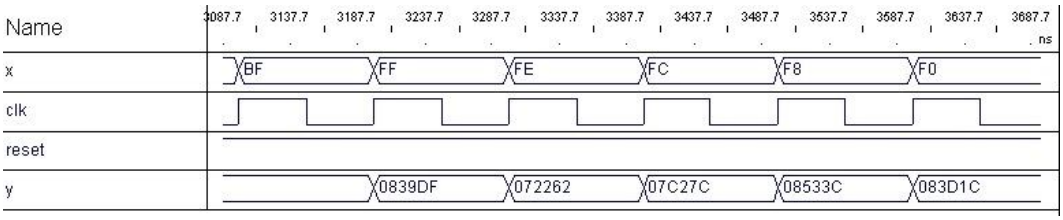

Figure 4(b): Simulation Results of Proposed LPTV filter

Both the designs are synthesized with Xilinx ISE10.1 and implemented on Virtex 2vp30-7ff896FPGA. The synthesis results are presented in Tables 1 and 2. Table 1 presents macro statistics of the proposed design. Table 2 gives the comparison between the two designs. The results show that the proposed design reduces the area complexity and also power consumption. The RTL schematic is shown in Figures 5.

Table 1: Macro Statistics

#ROMs	1
#LUT RAMs	32
# Adders/Subtractors	31
# xors	2272
# Registers	506
# FlipFlops/Latches	506
# Multiplexers	33
# IO Buffers	31
# BELS	5159

Table 2: Synthesis Results

	LPTV FIR Filter (Proposed realization)	LPTV FIR Filter (Conventional realization)
Number of Slices	2758 out of 13696 (20%)	3560 out of 13696 (26%)
Number of slice Flip-Flops	266 out of 27392 (0%)	365 out of 27392 (1%)
Number of 4 input -LUTs	4876 out of 27392 (12%)	4695 out of 121504 (17%)
Number of Bonded IOBs	32 out of 556 (5%)	32 out of 556 (5%)
Number of Global Clocks	1 out of 32(3%)	1 out of32(3%)
Estimated power consumption	120mw	224mw

V. CONCLUSION

We developed an area efficient LPTV filter architecture using the output switching representation. It is realized by using a single LTI filter architecture along with distributed coefficient banks. We reduced the number of multipliers and there by reduced the area complexity. The proposed architecture consists of *N* multipliers for its realization whereas the conventional implementation needs *MN* multipliers. The proposed design is simulated synthesized and implemented on Virtex 2vp30-7ff896 FPGA. The results show that the proposed architecture reduces the area complexity and power consumption compared to the conventional implementation of LPTV FIR filter in output switching representation.

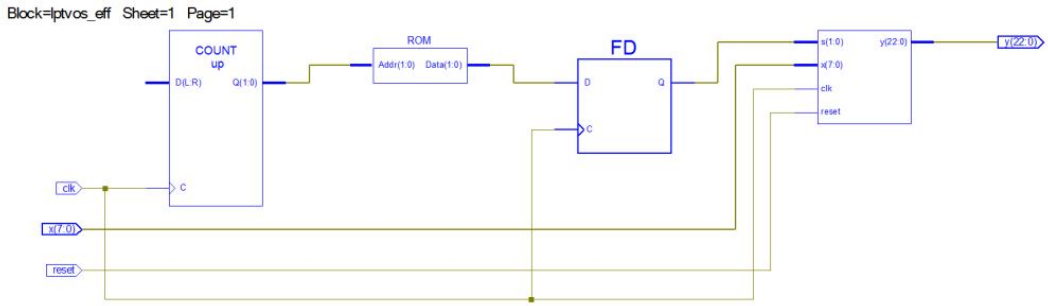

Figure 5: RTL Schematic of Proposed LPTV filter

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