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Behavioural Modelling and Simulation of PLL Based Integer N Frequency Synthesizer using Simulink

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Abstract

Behavioural modeling and simulation of a PLL based integer n frequency synthesizer has been illustrated in this paper. The synthesizer generates a signal of 5.15-5.25 GHz in the UNII (Unlicensed National Information Infrastructure) lower band which is used by IEEE 802.11(a). All the PLL building blocks are modeled and simulated using Simulink. The PLL performance has been evaluated using MATLAB. It is verified that the PLL loop bandwidth and phase margin are 0.25 MHz and 69.125 degree respectively, which satisfies the correct transfer function. Simulation results of the integer frequency synthesizer confirm the validation of the model.

Keywords: Phase frequency detector, Voltage controlled oscillator, Loop filter, Programmable divider, Simulink

Introduction

The phase locked loop (PLL) is a closed loop control system that has the ability to generate a feedback signal whose phase and frequency are aligned to the phase and frequency of the reference signal at locked condition [1-3]. The charge pump phase-locked loop (CPPLL) is widely used for its frequency sensitive error signal, as it can aid acquisition when the loop is out of lock [1].It consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF) and a voltage controlled oscillator (VCO) in the forward path and a frequency divider (FD) in the reverse path. When the PLL is in lock, there is a small phase difference between the two input signals of the phase frequency detector [2]. According to that error signal, the CP either increases or decreases the amount of charge to the LF. This amount of charge either speeds up or

slows down the VCO and shifts the VCO from its free running frequency and keeps the loop in lock [3]. The PLL technology has been widely used in many industries and research areas like wireless communication, cordless phone, home automation and global positioning systems.

The dual modulus prescaler based programmable frequency divider circuit has been implemented for the frequency synthesizer purpose which is shown in Figure 1. It consists of mainly three building blocks which are: dual modulus prescaler (*P*/*P*+1), swallow counter (*S*) and main counter (*M*).

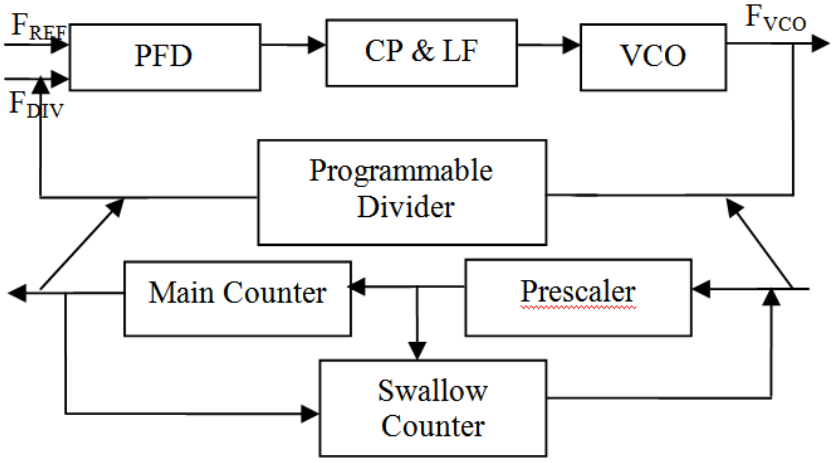


Figure 1: Integer N Frequency Synthesizer Architecture

The operation of the programmable divider is as follows

Initially the main counter and the swallow counter are loaded with the values *M* and *S* respectively, where *M* > *S* and *S* is externally controlled. The output of the swallow counter generates a load signal" /*lo*" and depending upon the load signal, the VCO signal is either divided by *P*+1 or *P*. When the */lo*=1, it divides by *P*+1 and when /*lo*=0, the VCO signal is divided by *P*. Hence, as long as the swallow counter is counting, the VCO signal is divided by *P*+1 and when it stops counting, the VCO signal is divided by *P*. The total number of input cycles counted by prescaler *P*+1 is *S* and that of *P* is *M*-*S*. Therefore, in the complete operation process, the total number of counts (*N*) is given by

$$N = (P+1)\,S + (M-S)\,P = MP + S. \quad (1)$$

In this paper, an integer n frequency synthesizer has been implemented which covers the UNII lower band. Now considering the frequency synthesizer for the UNII lower band, which has a frequency range of 5.15-5.25 GHz with a reference frequency of 5 MHz. Dividing the value of 5.15-5.25 GHz with 5 MHz, the total division factor lies between 1030 - 1050. Table 1 describes the most convenient values for designing the programmable divider.

Table 1: Programmable Divider Specification

Dual Modulus Prescaler (P/P+1)	32/33 (P=32)
Main Counter (M)	32
Swallow Counter (S)	6 - 26

The outline for the remainder of this paper is as follows. The frequency synthesizer building blocks are presented in Section 2. The PLL linear model is discussed in Section 3. Section 4 explains the simulation results and discussion. Finally, in Section 5, conclusion is given.

Frequency Synthesizer Building Blocks

The PLL based frequency synthesizer includes a phase frequency detector, a charge pump, a loop filter, a voltage controlled oscillator and a programmable divider. All the PLL building blocks are modeled and simulated using Simulink environment.

Phase Frequency Detector

The simulink model of the conventional sequential tri-states D flip-flop based PFD is shown in the Figure 2. A PFD with three states is widely used because of its wide linear range and ability to capture phase and frequency [1]. The reference signal and the feedback signal are given to the two input clock of the D flip-flop. The UP signal is created if the reference signal is faster than the feedback signal and DOWN signal is created if the reference signal is slower than the feedback signal. The UP and DOWN signals have no output signal when the reference and feedback signals are closed. This instant is known as dead zone condition. This problem can be avoided by using a delayed reset signal after the NAND gate as shown in the Figure 2. This delay in the reset path allows for both the UP and DOWN signals to activate the charge pump making the charge delivered to the loop filter proportional to the difference in duty cycle of these command signals [2].

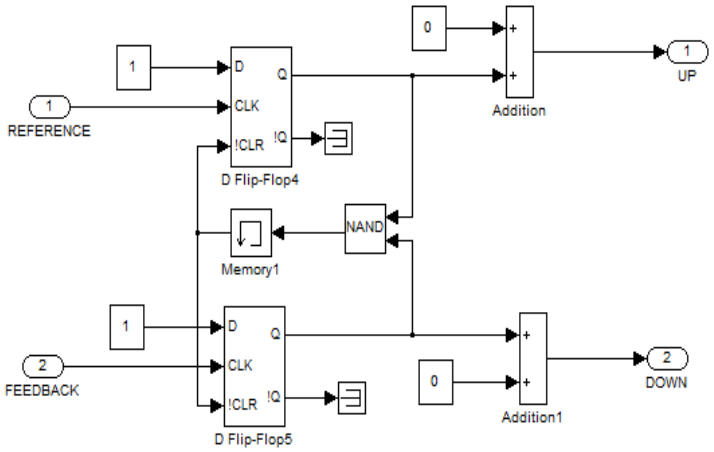


Figure 2: Building block of phase frequency detector

Charge Pump

The charge pump current drives the PFD output. It converts the output digital PFD signal into analog signal. The simulink model of the charge pump circuit is shown in the Figure 3 [4]. Basically, the charge pump consists of a current source, a current sink and two switches. However, the charge pump is usually followed by a passive loop filter that integrates the charge pump output current to a VCO control voltage. Thus, the charge pump output voltage is always equal to the VCO control voltage. The charge pump either sources or sinks current according to UP and DOWN signal. This amount of current is converted into controlled voltage by the loop filter for tuning the VCO [3]. To avoid current mismatching, the source and sink current values should be same. The control voltage increases when the reference signal leads the feedback signal and decreases when reference signal lags the feedback signal.

If the source and sink current of the charge pump are both I_{CP} the phase detector gain is given by

$$K_d = \frac{I_{\mathrm{CP}}}{2 \cdot \pi} \tag{2}$$

where K_d is the phase detector gain and I_{CP} is the charge pump current.

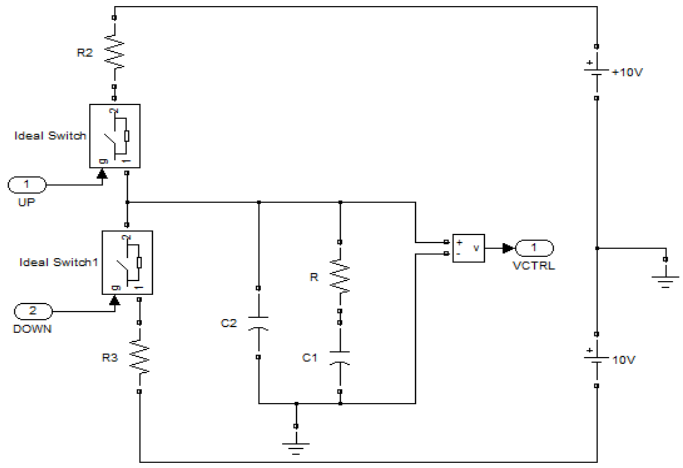


Figure 3: Building block of charge pump circuit

Voltage Controlled Oscillator

Generally the VCO is designed using CMOS technology. But in this paper, the behavioural VCO model has been implemented using simulink which is shown in the Figure 4. The VCO is designed by considering the basic mathematical formulas and design specification. The design specification for the UNII lower band frequency synthesizer is given in the Table 2. The simulation result of the VCO at locking position is shown in the Figure 5.

Table 2: Design specification for UNII band

Parameter	Specification
Frequency Range	5.15-5.25 GHz
Step Size	5 MHz
Voltage Range	0-2 V

The output frequency of VCO is adjustable by means of a controlled voltage V_{CTRL} such that

$$F_{\mathrm{VCO}} = F_0 + K_{\mathrm{VCO}} \times V_{\mathrm{CTRL}} \tag{3}$$

where, F_0 is the free running frequency at $V_{\mathrm{CTRL}} = 0$, K_{VCO} is the sensitivity/gain of VCO and V_{CTRL} is the controlled voltage.

The phase of the VCO can be calculated by integrating Equation (3) which is

$$\phi_{\mathrm{VCO}}(t) = \phi_0 + 2\pi \cdot K_{\mathrm{VCO}} \cdot \int V_{\mathrm{CTRL}}(t) \tag{4}$$

where ϕ_0 is the initial phase of the VCO.

The phase disturbances used in the PLL model can now be expressed using the VCO gain K_{VCO} which is

$$\phi_{\mathrm{VCO}}(\mathrm{t}) = 2\pi \cdot K_{\mathrm{VCO}} \cdot \int V_{\mathrm{CTRL}}(\mathrm{t}) \tag{5}$$

Laplace transform of Equation (5) gives the VCO transfer function as

$$\frac{\phi_{\mathrm{VCO}}(\mathrm{t})}{V_{\mathrm{CTRL}}(\mathrm{t})} = 2\pi \cdot \frac{K_{\mathrm{VCO}}}{\mathrm{s}} \tag{6}$$

The VCO sensitivity / gain can be calculated from the design specification in Table (2), which is

$$K_{\mathrm{VCO}} = \frac{f_{\max} - f_{\min}}{V_{\max} - V_{\min}} = \frac{5.25 - 5.15\mathrm{GHz}}{2 - 0\mathrm{V}} = 50\,\frac{\mathrm{MHz}}{\mathrm{V}} \tag{7}$$

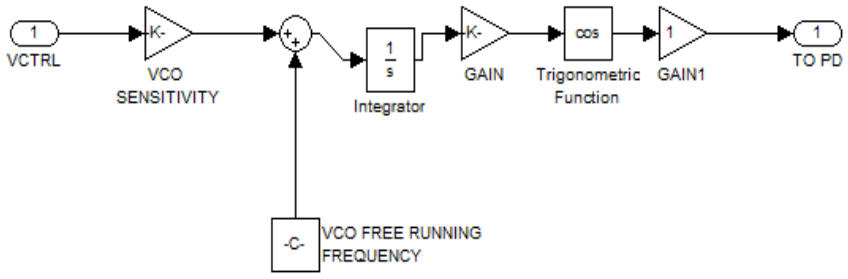


Figure 4: Simulink model of VCO

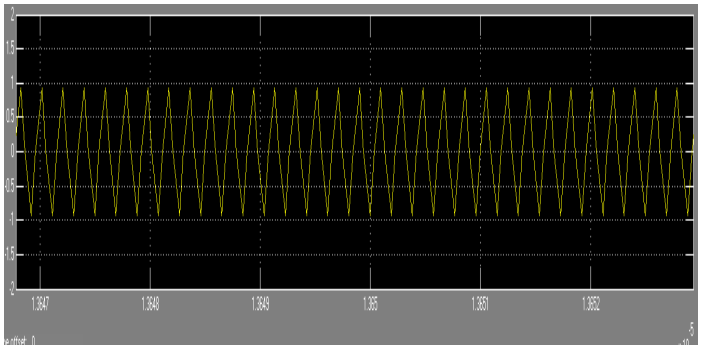


Figure 5: VCO simulation output at locking position

Programmable Divider

For high speed frequency synthesizer design, the circuit must incorporate high speed dual modulus or multi modulus divider [5]. In this paper, the dual modulus prescaler based programmable divider architecture has been implemented which is shown in the Figure 6. In this circuit, the output VCO signal is divided by the prescaler either *P*/*P*+1 depending upon the output of the swallow counter. Here, the swallow counter circuit [6] has been implemented.

The operational principle of the swallow counter is as follows:

Initially the swallow counter loads a value between 6 and 26. After that, it starts to count in descending manner up to zero. When the value zero is reached, the counter once again initializes the value and starts to decrement. In summary, when the "l*o/"*= 0, the values IA, IB, IC, ID, IE are loaded and when the "l*o/"*= 1, the values IA, IB, IC, ID, IE are decremented to zero.

The control logic operation of the programmable divider is as follows

When the outputs of the QA, QB, QC, QD & QE are zero, the OR output is zero. The swallow counter is initialized with the values IA…..IE and immediately, the OR output is forced to high. When the OR output is high, the VCO signal is divided by 33 prescaler units. The main counter output is still zero because the clock of swallow counter is connected to prescaler output. In every clock pulse, the main and swallow counter decrements their values to zero. At the instant the swallow counter stops counting, the OR output is zero and the VCO signal is divided by 32 prescaler units. Now the clock of the swallow counter is connected to the main counter output and its value is decremented from *M*-*S* to 0. When it reaches zero, the main counter stops counting. The operation is repeated after the counter is reset.

The simulation results of dual modulus prescaler output and swallow counter output for *S* = 16 and *N* = 1040 are shown in the Figurer 7 and 8 respectively. In Figurer 7, the upper one is VCO signal, middle one is load signal *"/lo"* and lower one is dual modulus prescaler output. Figure 8 shows, the QA to QE signals (top to bottom) for IA = low, IB = low, IC = low, ID = low and IE = high.

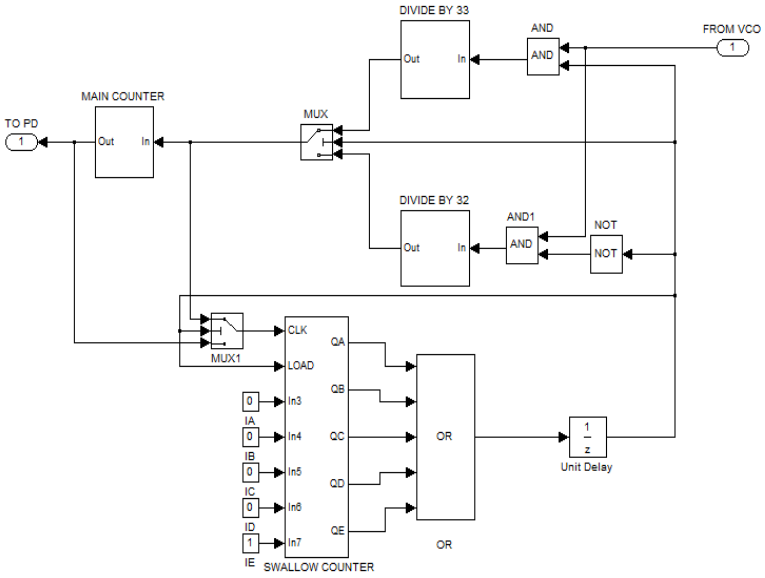


Figure 6: Dual modulus prescaler based programmable divider architecture

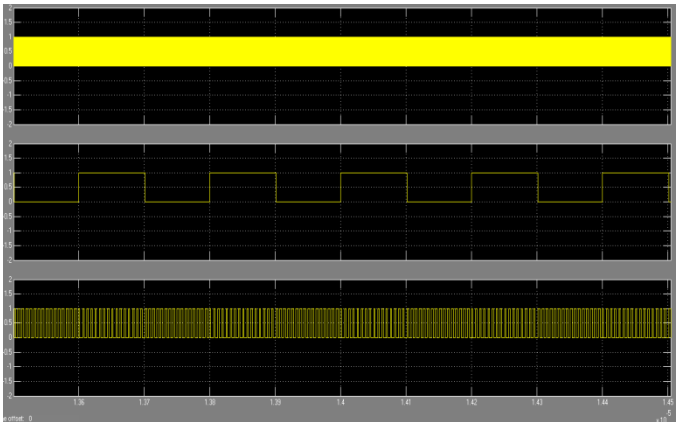


Figure 7: Dual modulus prescaler simulation results for S=16

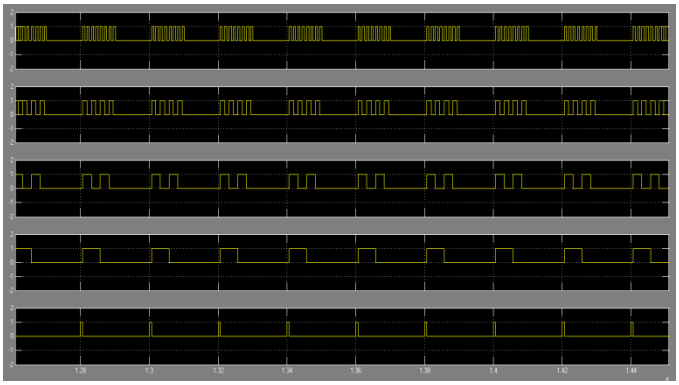


Figure 8: Swallow Counter Output for S=16 and N=1040

Loop Filter

The loop filter is the most important functional block as it evaluates the performance of the PLL. The filtering operation of the error voltage coming from the phase detector is performed by the loop filter. Basically the loop filter is non-linear system but can be seen as linear when it approaches lock. Figure 9 shows a 2nd order low pass filter. It has two poles and one zero. The zero is required in order to give sufficient phase margin and a stable PLL operation.

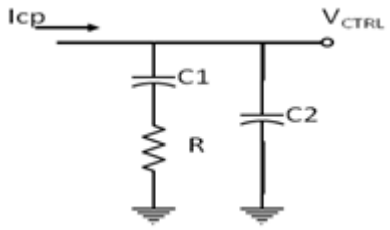


Figure 9: Second order loop filter

The transfer function of the 2nd order loop filter is given by

$$F(s) = \frac{V_{CTRL}(s)}{I_{CP}(s)} = R + \frac{1}{C1 \cdot s} \| \frac{1}{C2 \cdot s} \tag{8}$$

where V_{CTRL} is the voltage across the loop filter and I_{CP} is the current coming from the charge pump circuit.

After simplification of Equation (8), we get

$$\frac{R \cdot C1 \cdot s + 1}{R \cdot C1 \cdot C2 \cdot s^2 + s \cdot (C1 + C2)} = K_F \cdot \frac{s + w_Z}{s \cdot \left(\frac{s}{w_P} + 1 \right)} \tag{9}$$

Where $K_F = \dfrac{R \cdot C2}{C1 + C2}$

Thus, we can obviously acquire a zero w_Z and a pole w_P which are given by

$$w_Z = \frac{1}{R \cdot C1} \tag{10}$$

$$w_P = \frac{C1 + C2}{C1 \cdot C2 \cdot R} \cong \frac{1}{R \cdot C2} \tag{11}$$

To give the PLL correct bandwidth and phase margin, the loop-filter component values are adjusted. The detail calculations of the loop filter components value are described in the Section 3.

Pll Linear Model

Basically, PLL is a non-linear system, but can be seen as linear when it approaches locking position. Therefore, a PLL linear model should be considered. A linear model of a type -2, 3rd order charge pump PLL is shown in the Figure 10. It includes the phase frequency detector / charge pump gain K_d, the VCO gain $K_{VCO}(s)$, the loop filter transfer function $F(s)$ and the feedback path divider gain (N).

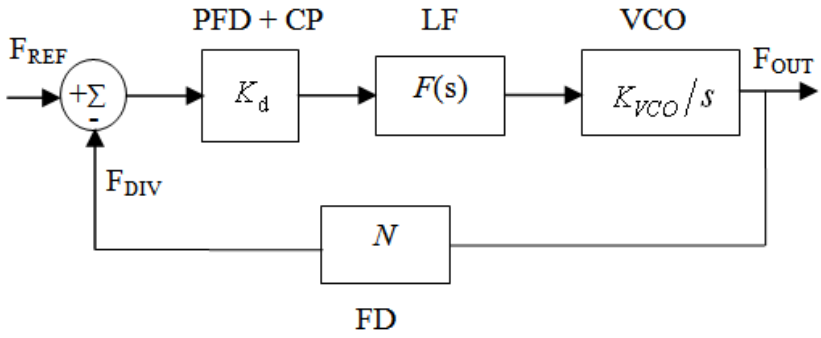


Figure 10: Linear PLL model architecture

The open loop transfer function of the third order PLL is given by

$$G(s) = \frac{K_d \cdot K_F \cdot K_{VCO}}{N} \cdot \frac{s + w_Z}{s^2 \cdot \left(s \cdot w_P^{-1} + 1\right)} \tag{12}$$

Typically, the value of charge pump current is taken to be 100 uA to 1 mA when off chip filter is used [7].

Phase margin is generally used for determination of system stability and is defined as the difference between 180 degree and the phase of the open loop transfer function at unit gain. To achieve PLL system stability, the phase margin should be at least or greater than 45 degree.

The phase margin (PM) of the loop at unit gain is given by

$$\varphi_P(w_C) = \tan^{-1}\left(\frac{w_C}{w_Z}\right) - \tan^{-1}\left(\frac{w_C}{w_P}\right) \tag{13}$$

By differentiating Equation (13) with respect to w_C and equating it to zero, the maximum phase margin can be achieved which is equal to

$$w_C = \sqrt{w_Z \cdot w_P} \tag{14}$$

To keep the system stable as well as for fast settling time, Equation (15) & (16) are to be satisfied [3].

$$w_Z = 4 \cdot w_C \tag{15}$$

$$w_p = 1/4 w_C \tag{16}$$

The gain cross over frequency of open loop PLL system after simplification of Equation (12) can be written as

$$w_C = \frac{K_d \cdot K_F \cdot K_{VCO}}{N} = \frac{I_{CP}}{2\pi} \cdot \frac{K_{VCO}}{N} \cdot \frac{R \cdot C2}{C1 + C2} \tag{17}$$

For system stability purpose, the open loop PLL bandwidth is taken to be at least or equal to the $1/10^{th}$ of the reference frequency [2]. Here, the loop bandwidth is taken to be $1/20^{th}$ of the reference frequency. Now, using Equation (15), (16), & (17), the R, C1 & C2 values are to be calculated. The values of the components used in this work are R = 276.125 KΩ,

C1 = 9.22 pF and C2 = 0.61 pF.

Results and Discussion

The integer n frequency synthesizer has been simulated using simulink. Table 3 shows the PLL parameter values used for simulation process. The bode diagram of open loop and closed loop PLL are shown in the Figure 11 (a) & (b) respectively.The result shows that the PLL loop bandwidth is 0.25 MHz and phase margin is 69.125 degree which indicates that the transfer function is working correctly and the system is stable.The locking waveforms of the frequency synthesizer are shown in the Figure 12(a) and 12(b) for S=16 and S=26 respectively.

Table 3: PLL parameter values for simulation process

Parameter	Value
Output Frequency	5.15-5.25 GHz
Reference Frequency	5 MHz
Loop Bandwidth	0.25 MHz
Phase Margin	69.125 degree
Control Voltage Range	0 – 2 V
Charge Pump Current	125 uA
VCO sensitivity	50 MHz/V
Series Resistance	276.125 KΩ
Series Capacitance	9.22 pF
Parallel Capacitance	0.61 pF

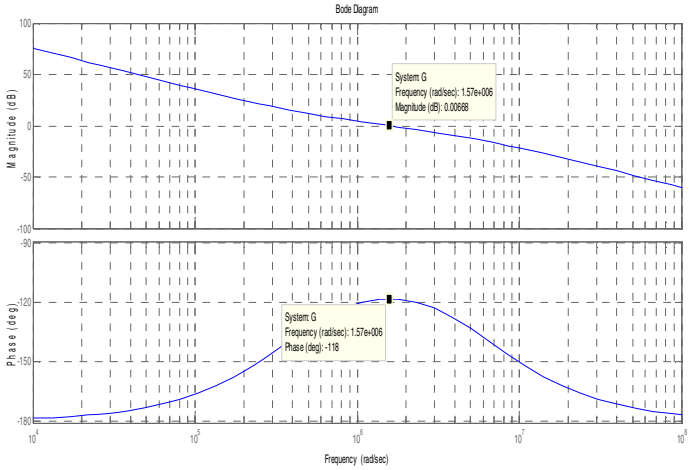


Figure 11: (a) Bode plot of open loop PLL

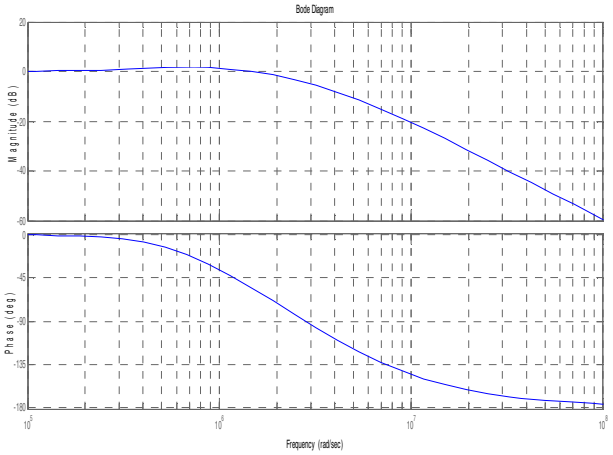
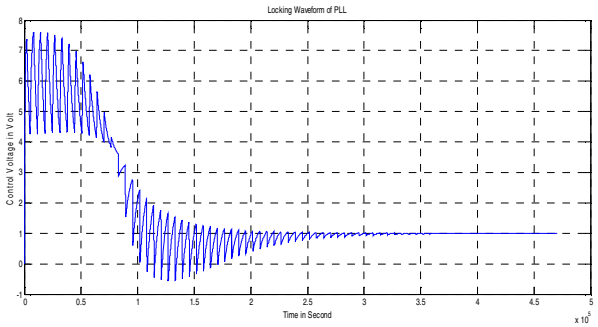
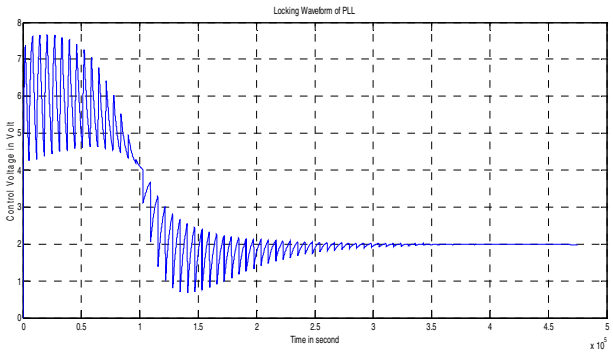


Figure 11: (b) Bode plot of closed loop PLL



(a)



(b)

Figure 12: Locking waveform of PLL (a) S=16 (b) S=26

Conclusion

In this paper, a PLL based integer n frequency synthesizer for UNII lower band covering a frequency range of 5.15-5.25 GHz has been simulated. The architecture is simple and the output frequency is varied integrally with the input reference frequency depending upon the channel selection of the programmable divider. The simulation has been done in SIMULINK platform. The simulation results shows that the PLL loop bandwidth and phase margin are 0.25 MHz and 69.125 degree respectively which indicates the correct transfer function. The PLL behaviour has been studied in broad sense and the performance has been evaluated using MATLAB. The results demonstrate the correct functioning of the model. We are investigating further to develop a model of the PLL system using CMOS technology.

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