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Implementation of Full Adder Cells using NP-CMOS and Multi-Output Logic Styles in 90nm Technology

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Abstract

In this paper we present two novel 1-bit full adder cells in dynamic logic style. NP-CMOS (Zipper) and Multi-Output structures are used to design the adder blocks. Characteristic of dynamic logic leads to higher speeds than the other standard static full adder cells. Using H-Spice and 90nm CMOS technology exhibits a significant decrease in the cell delay which can result in a considerable reduction in the power-delay product (PDP). The PDP of Multi-Output design at 1.8v power supply is around 0.15 fem to joule that is 5% lower than conventional dynamic full adder cell and at least 21% lower than other static full adders.

Index Terms: Style, Dynamic Logic, Full Adder, High Speed, Multi Output, NP-CMOS, Zipper.

Introduction

FULL Adder is the fundamental gate in many arithmetic circuits, such as adders and multipliers. Thus, enhancing the performance of the full adder block leads to the enhancement of the overall system performance [1], [2].Therefore, many efforts have recently done to implement high-speed and low-power 1-bit full adder cells with smaller area [10]-[20].A full adder cell is a three-input and two-output block in which the outputs are obviously the addition of three inputs. Adding two different numbers, A and B, ai and bi are the ith digit of the numbers. Carry input bit, Cin, derives from the previous block. The outputs, Sum and Cout, are the result of the sum operation. The functionality of a 1-bit full adder cell is:

$$Sum = A\ B\ Cin \quad (1)$$

$$Cout = A.B + A.Cin + B.Cin \quad (2)$$

Many approaches have been presented to decrease the total number of transistors to implement a given logic function such as pseudo-NMOS, pass-transistor logic, etc. The standard CMOS logic requires 2N transistors to implement an N input logic function, while pseudo-NMOS needs N+ 1 transistor. It has static power consumption due to its constant switched-on pull-up network. The disadvantage of pass- transistor logic is poor voltage levels and reduced noise margins. Dynamic is an alternative logic style to design a logic function. N+2 transistors are needed in this approach, N transistors to implement a pull-up or pull-down network and 2 transistors for the clock signal which is lower than static case. Some advantages of dynamic logic are: faster switching speeds, no static power consumption, non-ratioed logic, full swing voltage levels and less number of transistors [1].There is not any static power consumption in dynamic circuits. It only consumes dynamic power because no static path exists between VDD and GND. Higher speed is the major advantage of the dynamic logic design. Lower number of transistors per gate and absence of short circuit current are the reasons for faster switching speeds. The main drawback is higher power dissipation than static logic due to the higher switching activity. The average power consumption in a generic CMOS gate is measured by equation (3). Although the static power consumption does not exist, the overall dissipation can be higher when compared to a static logic gate. However, with high speed operation of dynamic logic, this drawback is negligible.

$$Pavg = Pdynamic + Pshort\text{-}circuit + Pstatic\text{-}\rightarrow \quad (3)$$

In this paper we present two novel single-bit full adder cells in dynamic logic style. One of them is introduced in NPCMOS (Zipper) logic and the other one in Multi-Output logic [3]. Both structures are optimized and tested separately in different voltages. Because of the dynamic mode, the speeds of the cells are much higher than the conventional static full adders in all voltages. A conventional dynamic and several standard static full adders are selected to be compared with: 1) The conventional dynamic full adder cell [1]. It has 16 transistors and is based on NP-CMOS logic style (Fig. 1). 2) The complementary pass-transistor logic (CPL) full adder [4], [5]. It has 32 transistors and is based on the CPL logic (Fig. 2).3) The conventional CMOS full adder [5]. It has 28 transistors and is based on the regular CMOS structure (Fig. 3).4) The transmission-gates CMOS (TGCMOS) full adder [6].It has 20 transistors and is based on transmission gates (Fig. 4).5) The low power implementation of the full adder cell which has 14 transistors (14T) [7]. This cell is based on transmission gates and the low power XOR design (Fig.5). 6) The transmission function full adder cell (TFA) [8]. It has 16 transistors and is based on the transmission function (Fig. 6).The rest of this paper is organized as follows: In Section II, we present our new designs. Then in Section III, the simulation results are shown. Finally, Section IV contains conclusion.

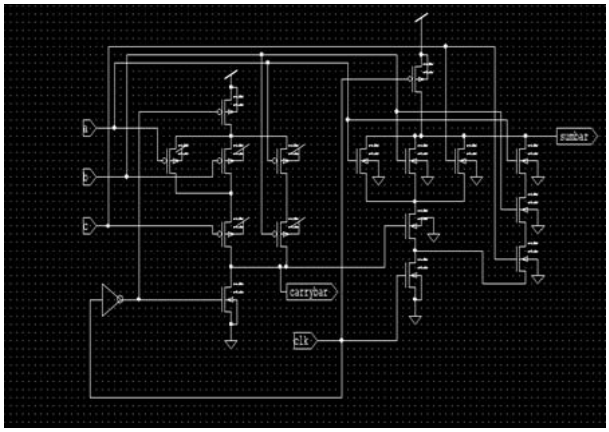

Figure 1: Conventional Dynamic Full Adder Cell

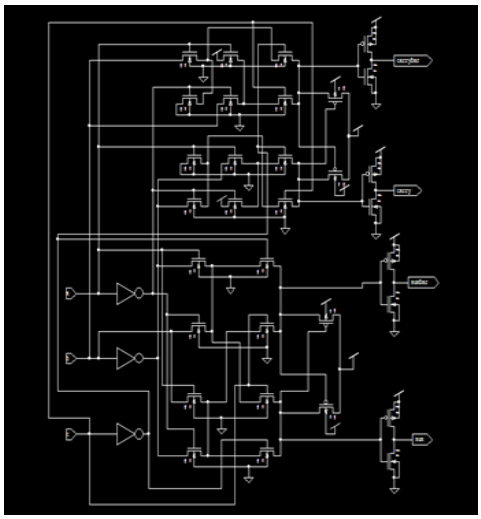

Figure 2: CPL

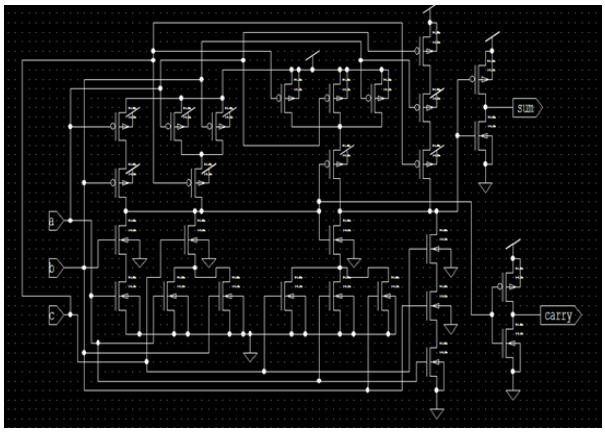

Figure 3: Conventional CMOS

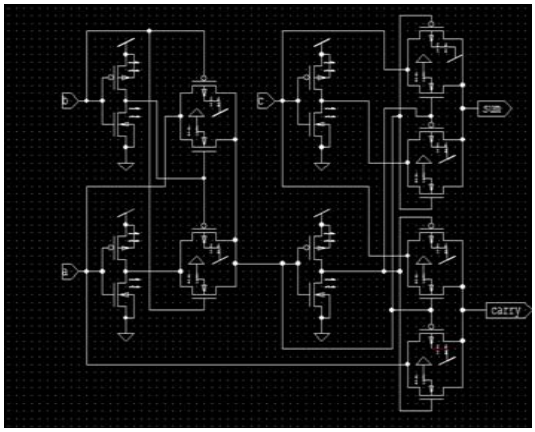

Figure 4: TGCMOS

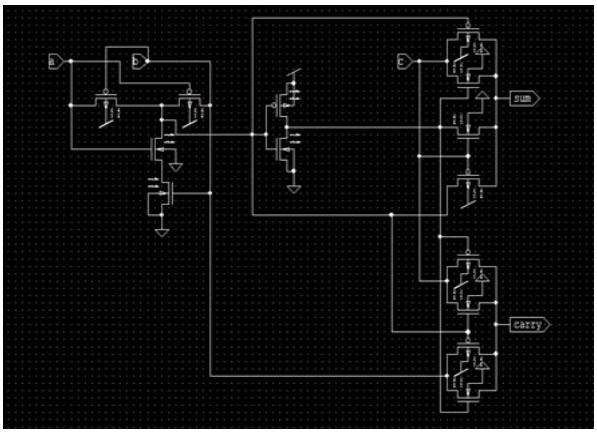

Figure 5: 14T

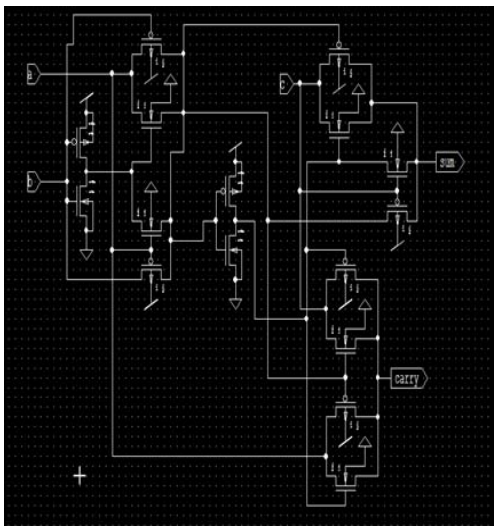

Figure 6: TFA

The Proposed Full Adder Cells

The First Design

Dynamic is an alternative logic style to design a logic function. It has some advantages in comparison with static mode such as faster switching speeds, no static power consumption, non-ratioed logic, full swing voltage levels and less number of transistors. For an N input logic function, it requires N+2 transistors versus 2N transistors in the standard CMOS logic. It only consumes the dynamic power. Finally high speed is the distinct specification of this logic style. There are two phases in dynamic logic. For a structure where output node is connected to VDD by a precharge PMOS transistor, there has to be a pull-down network implemented in NMOS. When Clock=0, circuit enters the precharge phase and when Clock=1, the evaluation phase starts. All the input values should be changed at precharge phase to avoid the charge sharing problem and incorrect functionality. It is because once the output discharges at evaluation phase, there will be no path between output and VDD to charge it again until the next precharge phase. The Sum output function can be described by the following Equation:

$$\text{Sum} = \text{out} = C \cdot (A + B + Cin) + A.B.Cin \dashrightarrow \quad (4)$$

One approach is to use NP-CMOS (Zipper) logic style to implement the 1-bit full adder cell (Fig. 7). At the first stage the out C function is obtained by using the bridge style [9]. At the second stage the Sum function is gained according to the equation (4).The first design has 16 transistors. It has full swing voltage levels. Clock and Clock' signals cause both stages of the circuit to enter the evaluation phase simultaneously.

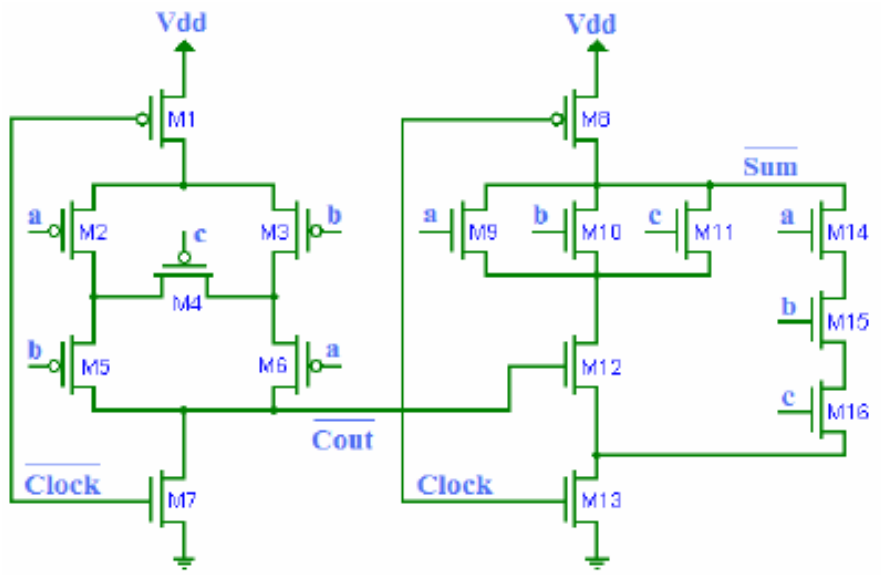

Figure 7: First Proposed Full Adder Cell Using NP-CMPS Dynamic Logic

The Second Design

Multi-Output dynamic logic is used to design the second circuit. The second design is introduced with the aim of enhancing the first design. The primary schema for the second design is shown in Fig. 8. Two PMOS transistors are used to charge the outputs in precharge phase. The bridge style is used to obtain out C and then, out C itself creates the Sum function. But there is a flaw which results in incorrect functionality. When the entire input signals equal to VDD, minterm A.B.Cin, there is a path that connects the GND to the Cout output (Fig. 8). The incorrect logical value of 0 is gained instead of logical value 1 as a result.

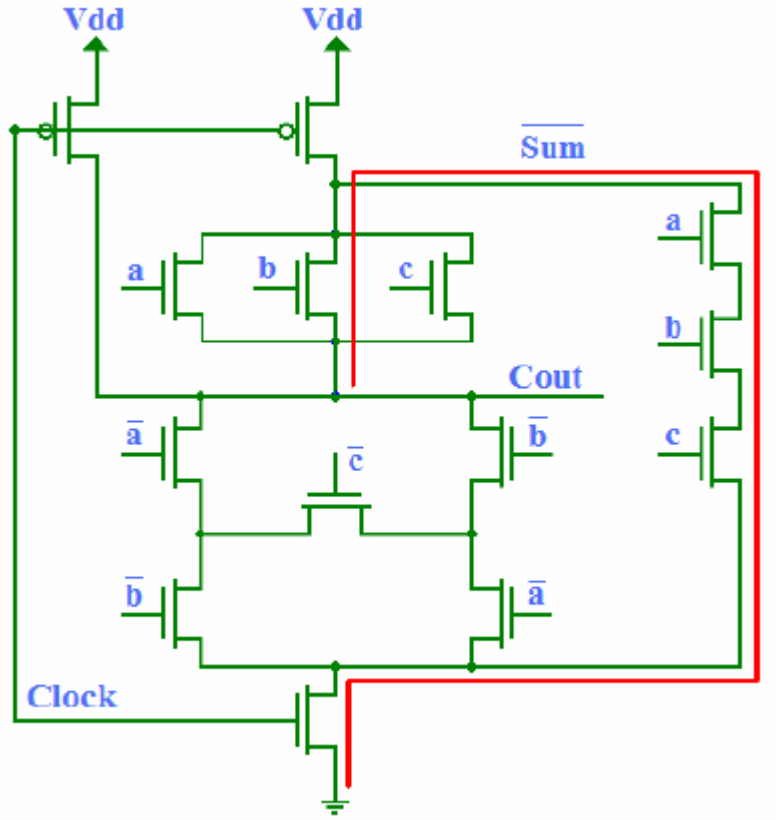

Figure 8: Primary Schema for the Second Design

To rectify the mentioned fault, the PMOS transistor M6 is added to avoid the incorrect result (Fig. 9). When the input pattern is A=B=Cin=1, the supplemented transistor switches off and intercepts the path between GND and Cout. In other min terms the existence of M6 does not affect the functionality of the circuit. Thus, by adding only one transistor the functionality of the cell is corrected.

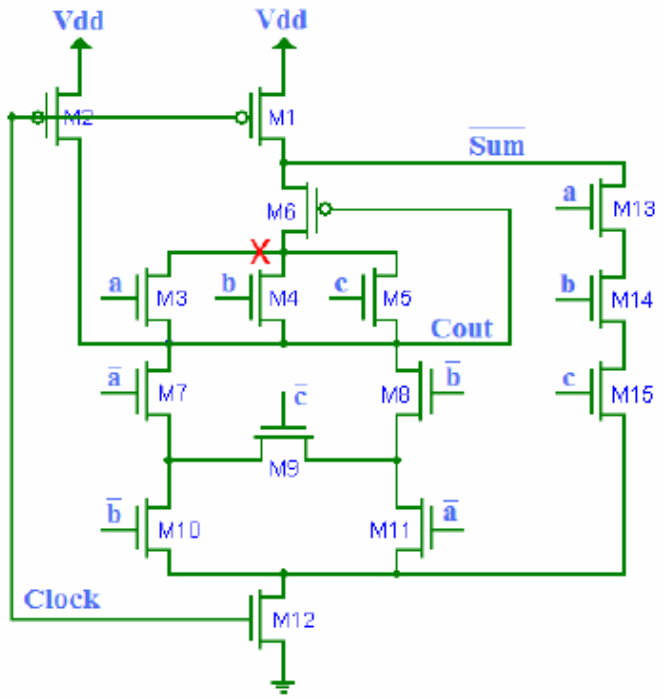

Figure 9: Modified Schema for the Second Design

The modified second design still has some weaknesses. First, it has charge sharing problem. When the circuit enters the evaluation phase, the existent capacitor at the node X (Fig.9) discharges the Sum output and leads to a voltage drop. The second problem occurs because of adding the PMOS transistor, i.e. the low level voltage is a little higher than 0v.The final schema of the second design is depicted in Fig.10. By exchanging the position of M6 with M3, M4 and M5,the charge sharing problem is eliminated considering the fact that the inputs should only be changed in precharge/predischarge phase. Therefore, we overcome the charge sharing problem without adding more transistors. Drain and Source of M6 are connected to each other. As a result, this transistor is either off or in saturation state. Hence, when the transistor is switched on, it operates like a resistance. Equation (5) shows the proportion of the impedance of a transistor to the width and the length of the

Channel:

$$Z = L / W \text{ ---}\rightarrow \quad (5)$$

Since L is the smallest possible technology size, enlarging the W parameter causes the equivalent impedance of M6 to decrease and the delay of the cell reduces subsequently. This also makes the low voltage level become even lower. Adding the transistors needed for the inverted inputs to the ones in the design, there will be totally 21 transistors.

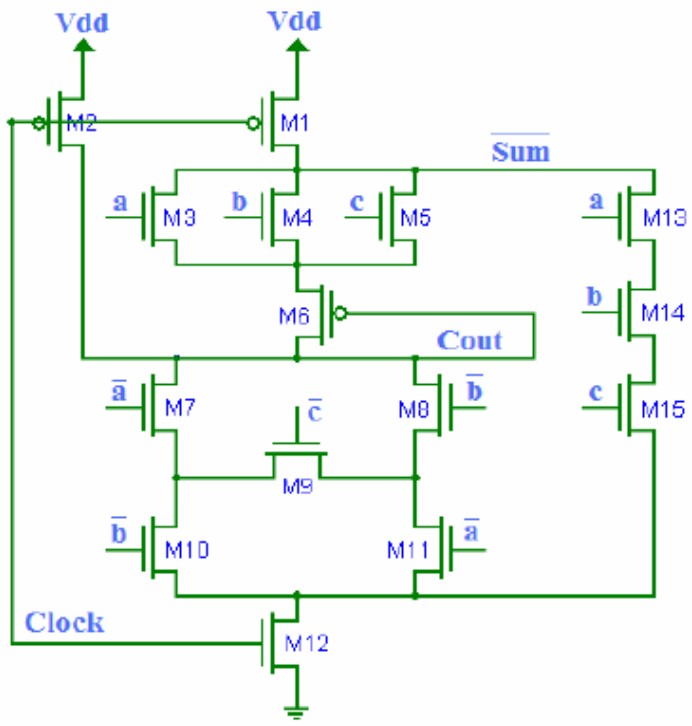

Figure 10: Final Schema for the Second Design Using Multi Output Dynamic Logic

The Simulation Results

Both proposed designs and the other six conventional full adder cells (Conventional Dynamic, Conventional CMOS, CPL, TGCMOS, 14T and TFA) are all simulated using HSpise and 0.18 m CMOS technology at room temperature. Because of dynamic logic characteristic, the inputs should be changed in precharge/predischarge phase and the results are obtained during evaluation phase. The output signals at the power supply of 1.8v are depicted in Fig. 11 for both proposed cells. The frequency of clock signal is 200MHz.The delay parameter is calculated from the time that the clock signal reaches 50% of the supply voltage level, to the time that the output reaches the same voltage. The falling propagation delay is separately measured for every output discharge and their maximum is reported as the delay of the cell. Since there is a precharge phase for the Sum output, the rising propagation delay equals zero. The average power consumption during all the transitions is considered as the power consumption parameter. Finally the power-delay product (PDP) is the multiplication of the maximum delay and the average power consumption as shown in equation (6).PDP = Max (Delay) * Avg (Power Consumption) (6) As dynamic power is proportional to VDD 2, lowering the power supply leads to less power dissipation. Hence, simulation is done for a various range of voltages from 3.3v to 0.8v. Although high power consumption can be a drawback of dynamic logic, it is still less than some other static full adder cells. The results for delay, power consumption and PDP parameters are separately illustrated in Fig. 12, Fig. 13 and Fig. 14 respectively.

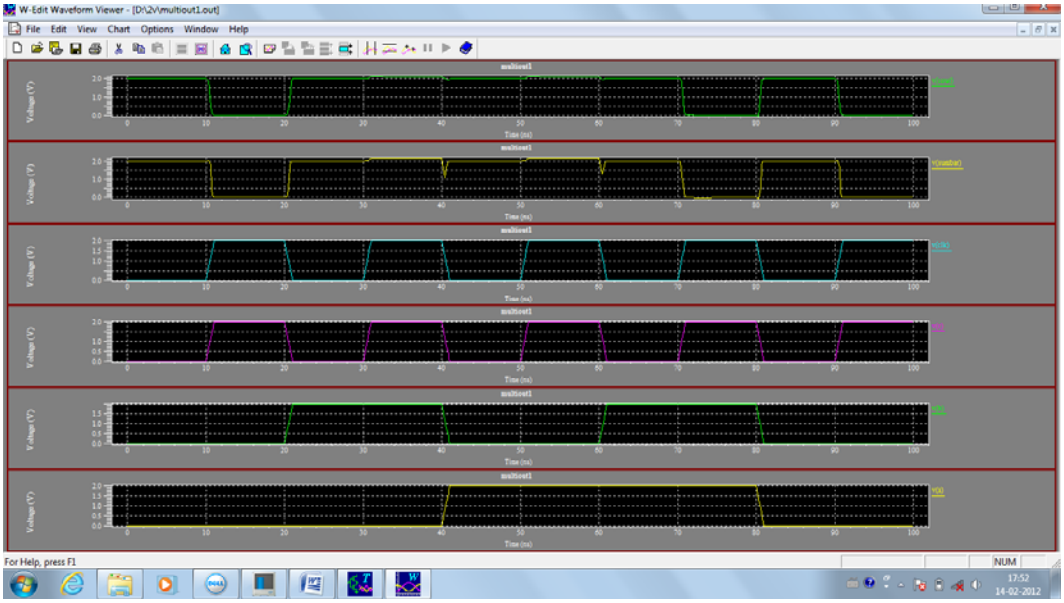

Figure 11: Input and Output Signals for Both Designs at 1.8v (Vertical Axis is Voltage & Horizontal Axis is Time)

The results are shown in Table I at 0.8v, 1.2v and 1.8v.Using 1.8v power supply, the first design is 94% faster than Conventional CMOS, 41% faster than 14T, 26% faster than TGCMOS, 25% faster than CPL and 12% faster than TFA. It consumes 166% less power than CPL, 23% less than TGCMOS and 13% less than Conventional CMOS. The PDP is 232% lower than CPL, 119% lower than Conventional CMOS, 54% lower than TGCMOS, 29% lower than 14T and 1% lower than TFA.The results of the second design are much better than the first one so that in 1.8v power supply, it is 120% faster than Conventional CMOS, 59% faster than 14T, 42% faster than CPL and TGCMOS, 27% faster than TFA and 2% faster than Conventional Dynamic. It consumes 181% less power than CPL, 30% less than TGCMOS, 19% less than Conventional CMOS and 3% less than Conventional Dynamic. Finally its PDP is 298% lower than CPL, 163% lower than Conventional CMOS, 85% lower than TGCMOS, 55% lower than 14T, 21% lower than TFA and 5% lower than Conventional Dynamic.

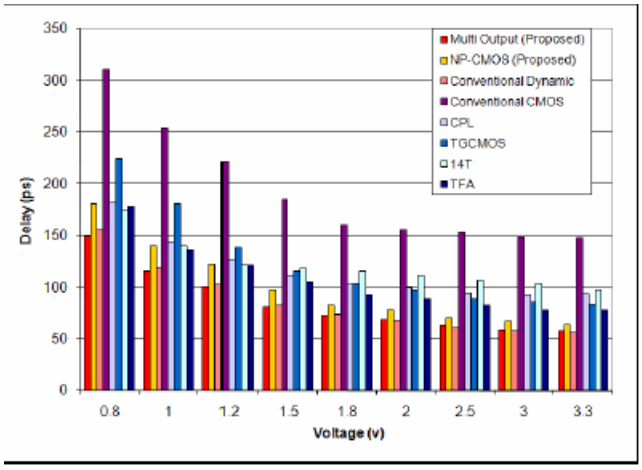

Figure 12: Delay of the Full Adder Cells, versus Supply Voltage

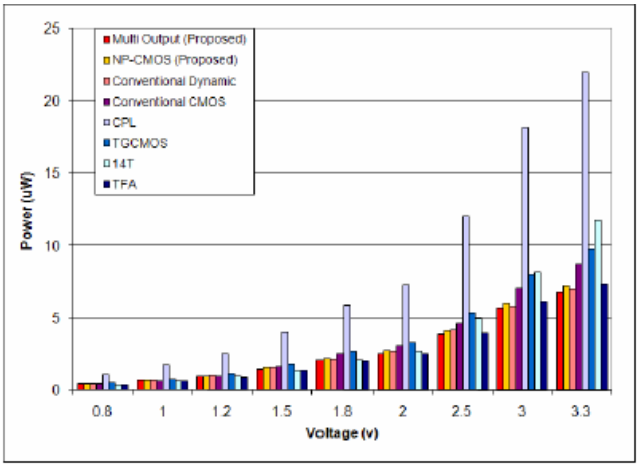

Figure 13: Power Consumption of the Full Adder Cells, versus Supply Voltage

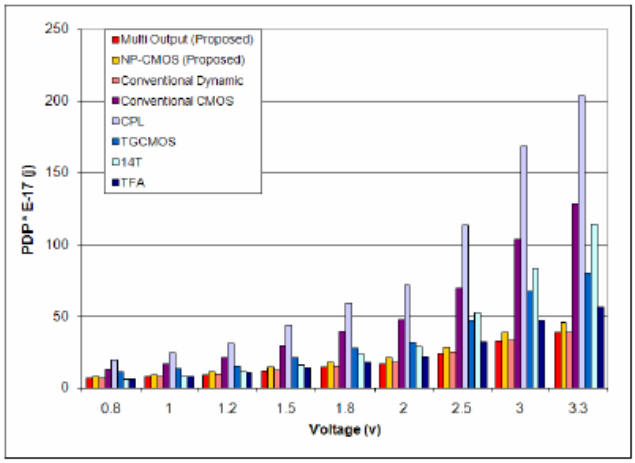

Figure 14: Power-Delay Product of the Full Adder Cells, versus Supply Voltage

Table 1: Comaparision of All Logic families at 1V

Model	Avg. Power Consumption (µw)	Delay (ns)	PDP* E-13(j)	EDP* E-22
Multi out (proposed)	1.73	0. 381	0.0065	0.00247
NP-CMOS (proposed)	1.67	9.91	0.165	1.63
Conventional Dynamic	1.98	9.91	0.196	1.94
Conventional CMOS	2.26	30.52	0.689	21
CPL	6.90	20.59	1.42	29.23
TGCMOS	1.92	30.09	0.57	17.15
14T	16.35	9.83	1.60	15.72
TFA	1.92	30.09	0.57	17.15

Conclusion

NP-CMOS and Multi-Output dynamic logic style have been used to design two novel high-speed full adder cells. Using HSpice and 0.18 m CMOS technology has revealed that the Multi-Output structure has much better performance than the other conventional static and dynamic cells. However, the power consumption is a weakness of dynamic logic, but our structures consume less power than other static cells at many voltages. The PDP of the second design is 298% lower than CPL, 163% lower than Conventional CMOS, 85% lower than TGCMOS, 55% lower than 14T, 21% lower than TFA and 5% lower than Conventional Dynamic. There was incorrect functionality in the primary schema of the Multi-Output design. After making some modifications the functionality was corrected, but still there were some drawbacks such as charge sharing problem and non-full swing voltage levels. In the final design, the charge sharing problem has been eliminated and the voltage levels have considerably been enhanced. It is worth working further on dynamic logic in the future because of its several advantages.

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