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Design Consideration and Effect of Parameter Variation on sub-40nm Bulk MOSFET using TCAD Tool

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Abstract

The scaling of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) has been governed over past several decades and is now becoming very critical due to its scaling limit and its short channel effects (SCE).In this paper several design consideration and the effects of various process parameters variation on the device performance is carried out for sub-40nm engineered MOSFET. Virtual Fabrication of sub-40nm Bulk MOSFET is carried out under channel engineering and source drain engineering process. These structures enable more aggressive device scaling in nano-scale region because of their ability to control short channel effects. How ever during scaling the junction depth should also be scaled down, which increases parasitic resistance so silicidation technique has been applied to reduce their effects on device. The variation of process parameters such as effects of well implantation, epitaxial doping, channel doping, oxide thickness and channel length on threshold voltage on device performance is carried out and also source drain concentration, and implantation energy on its junction depth and the effect of annealing temperature on sheet resistance is also investigated. Silvaco TCAD Tool is used for Virtual fabrication and simulation. ATHENA process simulator is used for virtual fabrication and ATLAS device simulator is used for device characterization and to study the effects of different process parameters on the device performance

Introduction

The manufacturing of an integrated circuit is complex because it involves variety of processing materials in its fabrication process. Each of these steps are the potential source of parameters variation in its device performance. The variations of various processing parameters are its implantation energy, doping concentration, temperature processing, well implantation etc and how these parameters behaves and its effects in nano-scale region of MOSFET device which is engineered. In this paper these process parameters effects are studied to understand its behavior in nano-scale region and how it effects on the device performance mostly on its threshold voltage and of course in sub threshold region. As in the fabrication process of sub-40nm bulk MOSFET the advance fabrication steps is being carried out such as lightly doped on both source and drain side, double halo implantation, retrograde well, and since junction is shallow so silicidation process is also carried out on source and drain terminal to decrease its sheet resistance and how the annealing process effects its sheet resistance. Another important parameters are gate oxide reduction and reduction in channel length on its threshold voltage. The parameter called threshold voltage roll of is the key parameter mainly defines the variation of threshold voltage when the channel length is reduced that is if we increase the supply voltage then the effective channel length of the device gets reduced and hence it reduces its threshold voltage causes threshold voltage roll-of. The effect of gate oxide thickness on its threshold voltage is performed

Design Consideration

According to ITRS roadmap[2],a precisely controlled process flow for the incorporation of new materials in Si CMOS technology is crucial for nanoscale devices. Also,an increased functionality at low cost leads an excessive high packaging density for VLSI chips, leads to an aggressive scaling of MOSFETs[3,4].

In this paper by using TCAD simulator we have used advances fabrication process such as: lightly doped drain to reduce peak electric field and to provide shallow junctions adjacent to the channel increase device density, halo implantation is introduced in which the locally the high doping concentration in the channel near the source/drain junction is created [1,4] to reduce punch through and hence called punch through stopper, retrograded p-well is a form of vertical channel engineering is used to increase surface channel mobility, and since scaling the junction depth causes increase in its sheet resistances at source/ drain terminal so metal silicide ($TiSi_2$) is used to reduce the sheet resistance and then the effects of various process parameters on the device performance is investigated to show the improved performance in terms of short channel effects reduction, less dependency of threshold voltage on variation of supply voltage and hence channel length variations results in reduction in short channel effects. There are various process parameters that can effects on the device performance and few of these process parameters variations are investigated and studied to demonstrate how these parameters behaves and effects in nano-scale device. Few of these are variations are, implantation energy on junctions depth, annealing temperature on sheet resistance, channel doping and gate oxide thickness on its threshold voltage, etc..

Results and Discussions

The process simulation uses ATHENA as a simulator that provides general capabilities for numerical, physically based, two dimensional simulation of semiconductor processing. In process simulation, the result of an implantation step is mostly described by a so-called pearson function where as the diffusion equation is solved to derive the influence of an annealing step.

The process steps are taken from Table1 and from reference paper[3,4].The initial grid has to be defined before any further steps of the design. A fine grid exist to those area of simulation structure where ion implantation will occur, where p-n junction will be formed. A retrograded p-well implantation is done with BF_2 at 90kev at 950°C.Sio_2 is deposited at 650-750°C using thermal oxidation by decomposing TEOS for sacrificial cleaning called screening oxide and is latter removed[8]. As the device is scaled the thickness of gate oxide must be scaled in order to overcome short channel effect. So a gate oxide of 25A° is then grown which is shown in the result after simulation. A high dose of arsenic for NMOS is implanted with 50kev to build low resistance of source and drain region. Introduction of dopant atom into semiconductor is the only steps in changing the electrical property. The implantation damages the target and displaces many atom for each implanted ion. Annealing is required to repair lattice damage and put the dopant atom on substitutional site where they will be electrically active[7]. The resistivity of even heavily doped silicon is too large, in those case it is common to form metal silicide on top of the exposed silicon to reduce the resistivity. $TiSi_2$ is most desirable film for many application due to its low resistivity [3]. During silicide formation anneal, however leads to over growth of the silicide on top of the edge of the oxide. This growth can be minimized by first annealing at low temperature to form TiSi and high temperature RTA around 750°C to form silicide[7]. Final device structure of a 40nm of n-channel MOSFET is shown in Fig1.

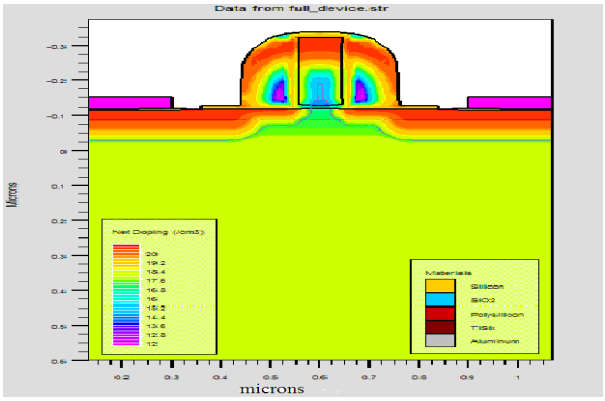

Figure 1: Device structure obtained ATHENA simulator.

Effect of well implantation on threshold

The well implantation has the effect of modifying its threshold voltage because as we

increases the concentration of p-type impurity along the channel the results in the increase in its threshold voltage shown in Fig2.

Table 1: Process Flow of 40nm NMOS used in SILVACO ATHENA process simulator.

Process	NMOS
Initial Substrate	p-type($2*10^{18}$per cm^3)
Epitaxial Layer	p-type($4*10^{16}$ per cm^3)
p-well implant	BF_2($1*10^{13}$), Energy=100kev
TEOS isolation and etch of oxide	10nm (diffusion at 650°C)
Gate oxide growth	2.5nm (At 650°C,dry o_2)
Poly deposition and etching for S/D	200nm (p-type $1*10^{15}$)
Shallow S/D implant	Phosphorus($8*10^{13}$,10kev)
Halo implant	p-type($1*10^{13}$), Energy=15kev/30° angle
Spacer deposition	100nm
Deep S/D implant	As($7*10^{14}$), Energy=50kev
Ti Silicide	25nm Ti on S/D and gate
Final RTA anneal	650-750°C for 30s and 1min
Metal deposition	Al-30nm

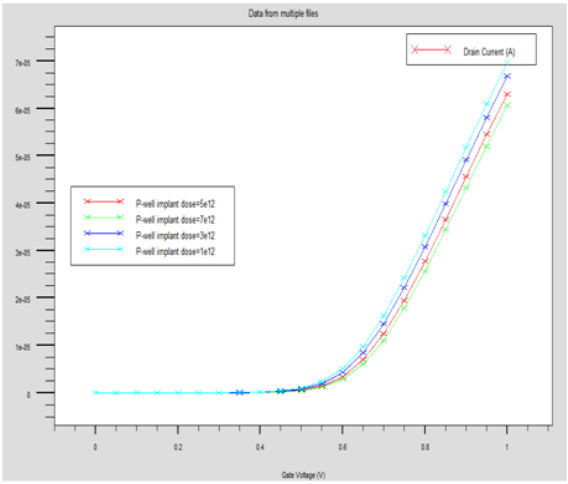

Figure 2: Well implantation Vs threshold voltage: showing slight variation on threshold voltage as we increase well implant.

Effect of epitaxial doping on threshold

As the concentration of epitaxial doping is increase from $1x10^{16}$ to $1x10^{17}$ then their threshold voltage also gets varied which is quite prominent and is shown in Fig3.

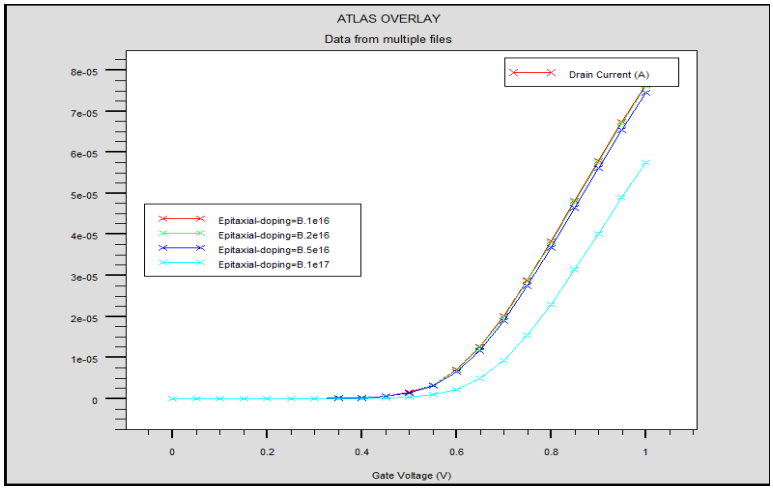

Figure 3: Epitaxial doping Vs Vgs for different doping concentration in ATLAS device simulator.

Effect of source/drain concentration on junction depth

If the concentration of arsenic is increased on both side of source/drain terminal then the junction depth is also gets increased and the depth of source/drain junction is measured for different doping concentration is shown in Fig4.

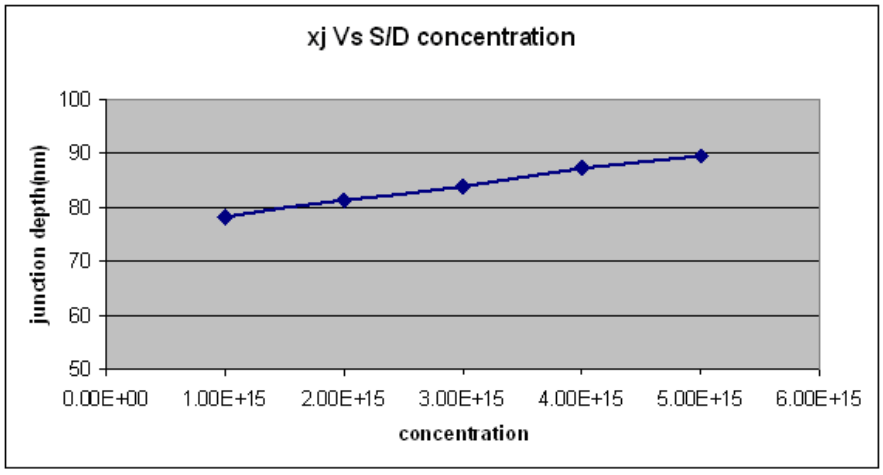

Figure 4: Junction depth Vs arsenic impurity Concentration.

Effect of implantation energy on Junction depth

An increase in the implantation energy on source/drain side has the effect of increasing the depth of the junction. So a proper choice of this implantation energy is must for a shallow junction and in this case it is 50kev and is varied to investigate its behavior which is shown in Fig5

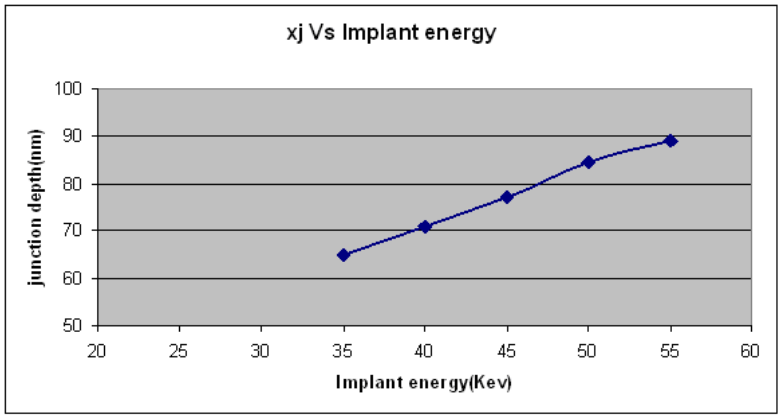

Figure 5: Junction depth for different implantation energy in Kev.

Effect of oxide thickness on threshold Voltage

The gate oxide thickness can be used to modify the threshold voltage of the transistor. Variation of threshold voltage with different oxide thickness for a 40nm device is shown in Fig6. Lower oxide thickness and hence lower the threshold voltage. Higher oxide thickness not only reduce the threshold leakage but it also reduces the gate oxide tunneling current, since the oxide the oxide tunneling current exponentially decreases with an increase in oxide thickness.

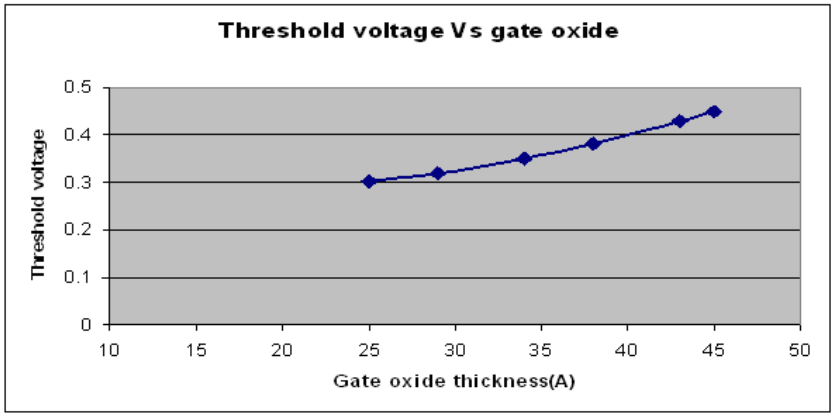

Figure 6: Variation of threshold voltage for different gate oxide thickness (Aº).

Effect of channel length on threshold Voltage

The threshold voltage decreases as the channel length is reduced. Hence different threshold voltage can be achieved by using different channel length. This reduction of threshold voltage with reduction of channel length is known as threshold voltage roll-off. It is clear from fig7 that there is less dependency of threshold voltage with variation in channel length shows improvement in short channel effect reduction.

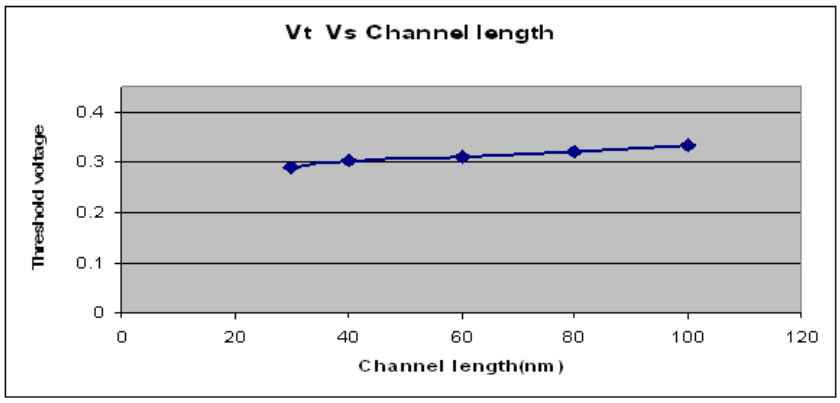

Figure 7: Threshold voltage (V) variation for different channel length (nm).

Effect of annealing temperature on sheet Resistance

Annealing is required to repair lattice damage and put the dopant atom on substitutional site where they will be electrically active. The annealing temperature has the effect on the sheet resistance is that as the as the annealing temperature increases then the sheet resistance is decreased which is quite prominent from the Fig8 shown below.

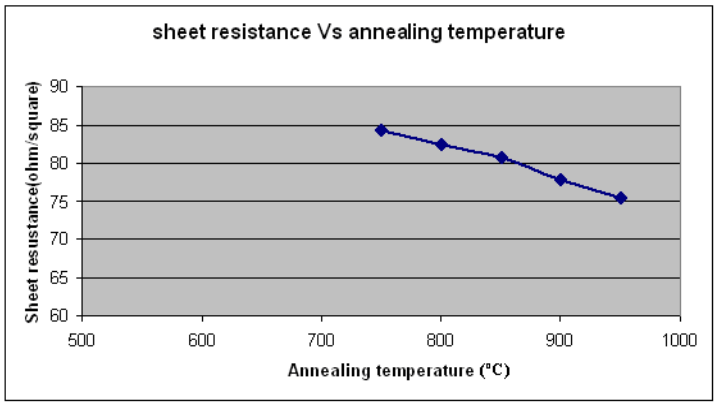

Figure 8: Annealing temperature Vs Sheet resistance.

Effect of channel doping on threshold Voltage

The channel doping depends on several components such as the type of atom being implanted, the dosage and the energy of the implant. The doping concentration and the depth are effected directly Multiple threshold voltage can be achieved by adjusting the channel doping. The threshold voltage increases as the channel doping increases which is comparable to the result reported in literature.

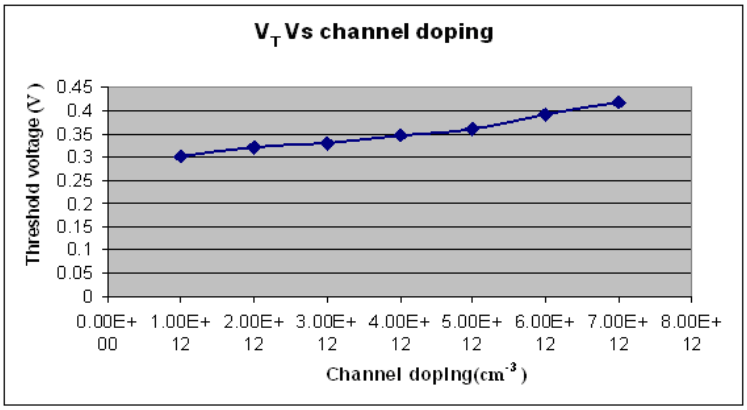

Figure 9: Threshold voltage for different Channel doping concentration.

Conclusion

The aim of this paper is to virtually fabricate a sub-40nm bulk MOSFET using advanced fabrication process and then a detail analysis of how the process parameters effects on its performance. A number of fabrication parameter that effects the value of threshold voltage, sheet resistance, junction depth on the device performance are investigated, and are optimizes for its better performance in terms of less dependency in threshold voltage while varying its channel length.

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