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A Multifunctional Cascaded Two-Level Inverter based STATCOM for DC-Link Voltage Balance in High Power Applications

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Abstract

In this paper An straightforward static var compensating plan utilizing a cascaded two-level inverter-based multilevel inverter may be suggested. The toponomy comprises from claiming two standard two-level inverters joined for course through open-end windings of a three-phase transformer. The dc-link voltages of the inverters need aid controlled at diverse levels with acquire four-level operation. Those execution of the multilevel STATCOM under adjusted What's more lopsided supply-voltage states would mimicked Previously, MATLAB. Further, solidness conduct of the toponomy may be investigated. Thedynamic model will be produced Also exchange works need aid determined. By using both animated Furthermore sensitive energy need favorable element through hysteresis passing Also secondary effectiveness. The framework conduct will be broke down for Different operating states.

Keywords: DC-link voltage balance, active power oscillation damping, flicker attenuation, multilevel inverter, power quality, static compensator (STATCOM).

I. INTRODUCTION

The application of Flexible ac transmission systems controllers such as static compensator and static synchronous series compensator is increasing in power systems. This is due to the relibility to stabilize the transmission systems and to improve the power quality in distribution systems. STATCOM is popularly accepted as a reliable reactive power controller replacing conventional var compensators, such as the thyristor switched capacitor and thyristor controlled reactor.

Generally in high power applications of var compensation is achieved using multilevel inverters. These inverters consist of a large number of dc sources which are usually realized by capacitors Hence, the converters drawa small amount of active power to maintain dc voltage of capacitors and to compensate the losses in the converter. However, due to mismatch in conduction and switching losses of the switching devices, the capacitors voltages are unbalanced. So by utilizing both active and reactive power losses are over come.

Cascade H-bridge is the most popular for static var compensation. The control of individual dc-link voltage of the capacitors is difficult. Static var compensation by cascading conventional multilevel two level inverters is an attractive solution for high-power applications. One of the advantages of this topology is that by maintaining asymmetric voltages at the dc links of the inverters the number of levels in the output voltage waveform can be increased.

The overall control is simple compared to conventional multilevel inverters. A three-level inverter and two-level inverter are connected on either side of the transformer low voltage winding. In three-level operation is obtained by using standard two-level inverters. The dc-link voltage balance between the inverters is affected by the reactive power supplied to the grid. The topology uses standard two-level inverters to achieve multilevel operation. The dc-link voltages of the inverters are regulated at asymmetrical levels to obtain four-level operation. To verify the efficacy of the proposed control strategy, the simulation study is carried out for balanced and unbalanced supply-voltage conditions.

From the detailed simulation, it is found that the dc-link voltages of two inverters collapse for certain operating conditions when there is a sudden change in reference current. In order to investigate the behaviour of the converter, the complete dynamic model of the system is developed from the equivalent circuit. The model is linearized and transfer functions are derived. Using the transfer functions, system behaviour is analysed for different operating conditions. By utilizing both active and reactive power the hysteresis losses are reduced and efficiency is increased.

II. CASCADED TWO-LEVEL INVERTER BASED MULTILEVEL STATCOM

Fig. 1 shows the power system model considered in this paper [6]. Fig. 2 shows the circuit topology of the cascaded two-level inverter-based multilevel STATCOM using

standard two-level inverters. The inverters are connected on the low-voltage (LV) side of the transformer and the high-voltage (HV) side is connected to the grid.

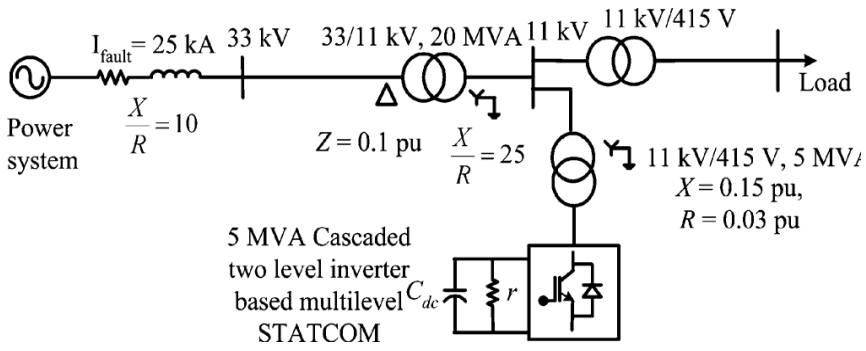

Fig.1: Power system and the STATCOM model

The dc-link voltages of the inverters are maintained constant and modulation indices are controlled to achieve the required objective. The proposed control scheme is derived from the ac side of the equivalent circuit which is shown in Fig. 3.

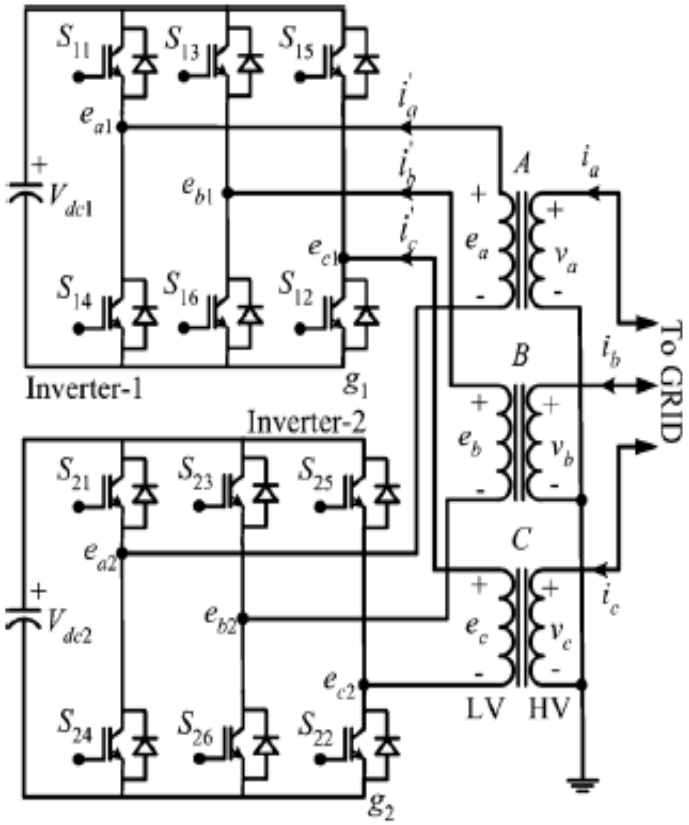

Fig.2: Cascaded two-level inverter based multilevel STATCOM

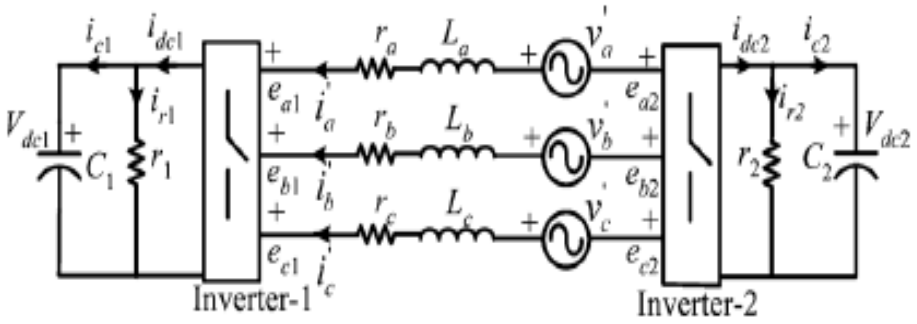

Fig.3: Equivalent circuit of the cascaded two-level inverter-based multilevel STATCOM.

In the figure v'_a,v'_b and v'_c are the source voltages referred to LV side of the transformer, r_a, r_b and $r_c$are the resistances which represent the losses in the transformer and two inverters, L_a, L_b and L_c are leakage inductances of transformer windings, and e_{a1}, e_{b1}, e_{c1}ande_{a2}, e_{b2}, e_{c2} are the output voltages of inverters 1 and 2, respectively. r_1, r_2 are the leakage resistances of dc-link capacitors $C_1$and C_2, respectively.

Assuming r_a= r_b= r_c= r, L_a= L_b=L_c= L and applying KVL on the ac side, the dynamic model can be derived using as

$$\begin{bmatrix} \frac{di'_a}{dt} \\ \frac{di'_b}{dt} \\ \frac{di'_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r}{L} & 0 & 0 \\ 0 & \frac{-r}{L} & 0 \\ 0 & 0 & \frac{-r}{L} \end{bmatrix} \begin{bmatrix} i'_a \\ i'_b \\ i'_c \end{bmatrix} + \frac{1}{L} \begin{bmatrix} v'_a - (e_{a1} - e_{a2}) \\ v'_b - (e_{b1} - e_{b2}) \\ v'_c - (e_{c1} - e_{c2}) \end{bmatrix} \tag{1}$$

Equation (1) represents the mathematical model of multilevel STATCOM in the stationary reference frame. This model is transformed to the synchronously rotating reference frame. The d-q axes reference voltage components of the converter$e_d^*$and $e_q^*$are controlled as

$$e_d^* = -x_1 + \omega L i'_q + v'_d \tag{2}$$

$$e_q^* = -x_2 - \omega L i'_d + v'_q \tag{3}$$

The synchronously rotating frame is aligned with source voltage vector so that the q-component of the source voltagev'_q is made zero. The control parameters$x_1$andx_2 are controlled as follows

$$x_1 = \left(k_{p1} + \frac{k_{i1}}{s} \right) \left(i_d^* - i'_d \right) \tag{4}$$

$$x_2 = \left(k_{p2} + \frac{k_{i2}}{s} \right) \left(i_q^* - i_q' \right) \tag{5}$$

The d-axis reference current i_d^* is obtained as

$$i_d^* = \left(k_{p3} + \frac{k_{i3}}{s} \right) \left[\left(v_{dc1}^* + v_{dc2}^* \right) - \left(v_{dc1} + v_{dc2} \right) \right] \tag{6}$$

The q-axis reference current $i_q^*$is obtained either from an outer voltage regulation loop when the converter is used in transmission-line voltage support [5] or from the load in case of load compensation.

A. Control Strategy

The control block diagram is shown in Fig. 4. The unit signals $\cos \omega t$ and $\sin \omega t$ are generated from the phase-locked loop (PLL) using three-phase supply voltages. The converter currents are transformed to the synchronous rotating reference frame using the unit signals.

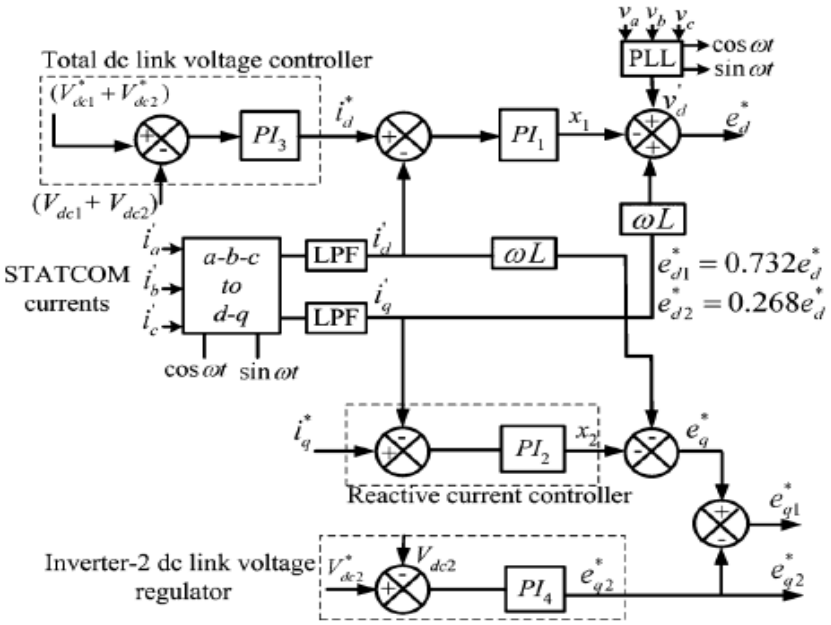

Fig.4: Control block diagram

The switching frequency ripple in the converter current components is eliminated using a low-pass filter (LPF). From $(v_{dc1}^* + v_{dc2}^*)$ and i_q^* loops the controller generates d-q axes reference voltages, e_d^* and e_q^* for the cascaded inverter. With these reference voltages, the inverter supplies the desired reactive current and draws required active current to regulate total dc-link voltage $v_{dc1}^* + v_{dc2}^*$. However, this will not ensure that individual dc-link voltages are controlled at their respective

reference values. Hence, additional control is required to regulate individual dc-link voltages of the inverters.

B. DC-Link Balance Controller

The resulting voltage of the cascaded converter can be given as $e_1\angle\delta$ where $e_1 = \sqrt{e_d^2 + e_q^2}$and $\delta = \tan^{-1}(e_q|e_d)$. The active power transfer between the source and inverter depends on δ and is usually small in the inverters supplying var to the grid [1]. Hence δ can be assumed to be proportional toe_q. Therefore the q-axis reference voltage component of inverter-2 e_{q2}^* is derived to control the dc-link voltage of inverter-2 as

$$e_{q2}^* = \left(k_{p4} + \frac{k_{i4}}{s}\right)\left(v_{dc2}^* - v_{dc2}\right) \tag{7}$$

The q-axis reference voltage component of inverter-1 e_{q1}^* is obtained as

$$e_{q1}^* = e_q^* - e_{q2}^* \tag{8}$$

The dc-link voltage of inverter-2 v_{dc2} is controlled at 0.366 times the dc-link voltage of inverter-1v_{dc1} [9]. It results in four-level operation in the output voltage and improves the harmonic spectrum. Expressing dc-link voltages of inverter-1 and inverter-2 in terms of total dc-link voltage v_{dc} as

$$v_{dc1} = 0.732 v_{dc} \tag{9}$$

$$v_{dc2} = 0.268 v_{dc} \tag{10}$$

Since the dc-link voltages of the two inverters are regulated the reference d-axis voltage component e_d^* is divided in between the two inverters in proportion to their respective dc-link voltage as

$$e_{d1} = 0.732 e_d^* \tag{11}$$

$$e_{d2} = 0.268 e_d^* \tag{12}$$

C. Unbalanced Conditions

Network voltages are unbalanced due to asymmetric faults or unbalanced loads. As a result, negative-sequence voltage appears in the supply voltage. This causes a double supply frequency component in the dc-link voltage of the inverter. This double frequency component injects the third harmonic component in the ac side. Moreover, due to negative-sequence voltage, large negative-sequence current flows through the inverter which may cause the STATCOM to trip. Therefore, during unbalance, the inverter voltages are controlled in such a way that either negative-sequence current flowing into the inverter is eliminated or reduces the unbalance in the grid voltage. In

the latter case, STATCOM needs to supply large currents since the interfacing impedance is small. This may lead to tripping of the converter.
The negative sequence reference voltage components of the inverter e_{dn}^{*} and e_{qn}^{*} are controlled similar to positive-sequence components in the negative synchronous rotating frame as

$$e_{dn}^{*} = -x_3 + (-\omega L) i_{qn}^{'} + v_{dn}^{'} \tag{13}$$

$$e_{qn}^{*} = -x_4 - (-\omega L) i_{dn}^{'} + v_{qn}^{'} \tag{14}$$

Where $v_{dn}^{'}, v_{qn}^{'}$ are d-q axes negative-sequence voltage components of the supply i_{qn}^{*} and i_{dn}^{*} are d-qaxes negative-sequence current components of the inverter, respectively. The control parameters x_3 and x_4 are controlled as follows

$$x_3 = \left(k_{p5} + \frac{k_{i5}}{s} \right) \left(i_{dn}^{*} - i_{dn}^{'} \right) \tag{15}$$

$$x_4 = \left(k_{p6} + \frac{k_{i6}}{s} \right) \left(i_{qn}^{*} - i_{qn}^{'} \right) \tag{16}$$

The reference values for negative sequence current components i_{dn}^{*} and i_{qn}^{*} are set at zero to block negative-sequence current from flowing through the inverter.

III. STABILITY ANALYSIS

Considering the dc side of the two inverters in the complete dynamics of the system are derived in the Appendix. The transfer function $\Delta\hat{v}_{dc1}(s)/\Delta\hat{v}\delta_1(s)$ is as follows and the transfer function $\Delta\hat{v}_{dc2}(s)/\Delta\hat{\delta}_2(s)$ is

$$\frac{\Delta\hat{v}_{dc1}(s)}{\Delta\hat{\delta}_1(s)} = \frac{num_1(s)}{den(s)} \tag{17}$$

$$\frac{\Delta\hat{v}_{dc2}(s)}{\Delta\hat{\delta}_2(s)} = \frac{num_2(s)}{den(s)} \tag{18}$$

The transfer function $\Delta\hat{v}_{dc1}(s)/\Delta\hat{v}_{\delta 1}(s)$ for $i'_{qo} = 1.02$p.u., (capacitive mode), it can be observed that all poles as well as all zeros lie on the left half of the s-plane for this operating condition. Fig.3. shows the frequency response of the transfer function $\Delta\hat{v}_{dc1}(s)/\Delta\hat{v}_{\delta 1}(s)$ for the same operating condition. From the figure, it can be observed that the system has sufficient gain and phase margins for this operating condition. An enlarged root locus of the transfer function $\Delta\hat{v}_{dc1}(s)/\Delta\hat{v}_{\delta 1}(s)$ when STATCOM is in inductive mode of operation. The reactive component i'_{qo} is set at 0.75p.u. and proportional gain k_p is varied from 0 to 10. It can be seen that all poles

lie on the left half of the s-plane for this case as well. However, one zero shift to the right half and three zeros lie on the left half of the plane. Moreover it can be seen that closed-loop poles of the system shift to the right half of the s-plane for high controller gains.

IV. SIMULATION RESULTS

The system configuration shown in Fig. 1 is considered for simulation. The simulation study is carried out using MATLAB/SIMULINK. The system parameters are given in Table I.

Table I: Simulation System Parameters

Rated power	5MVA
Transformer voltage rating	11KV/400
AC Supply frequency f	50Hz
Inverter-1 DC link voltage v_{dc1}	659 V
Inverter-2 DC link voltage v_{dc2}	241 V
Transformer leakage resistance x_1	15%
Transformer resistance R	3%
DC link capacitances $c_1 . c_2$	50 Mf
Switching frequency	1200Hz

A. Reactive Power Control

As reactive power is directly injected into the gridby setting the reference reactive current component i_q^* at a particular value. Initially, i_q^* is set at 0.5p.u. At t=2.0 s, i_q^* is changed to 0.5 p.u. Fig. 5 shows the source voltage and converter current of the A phase. Fig. 6 shows the dc-link voltages of two inverters. From the figure, it can be seen that the dc-link voltages of the inverters are regulated at their respective reference values when the STATCOM mode is changed from capacitivet inductive. Moreover, the dc-link voltage of inverter 2 attains its reference value faster compared to that of inverter 1. The reactive power has an advantage over hysteresis loss and has good efficiency.

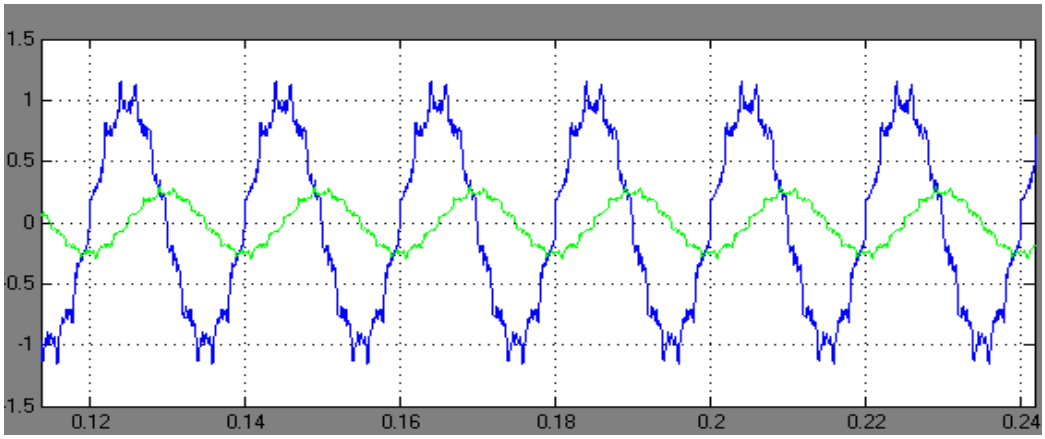

Fig. 5: Reactive power control of Source voltage and inverter current.

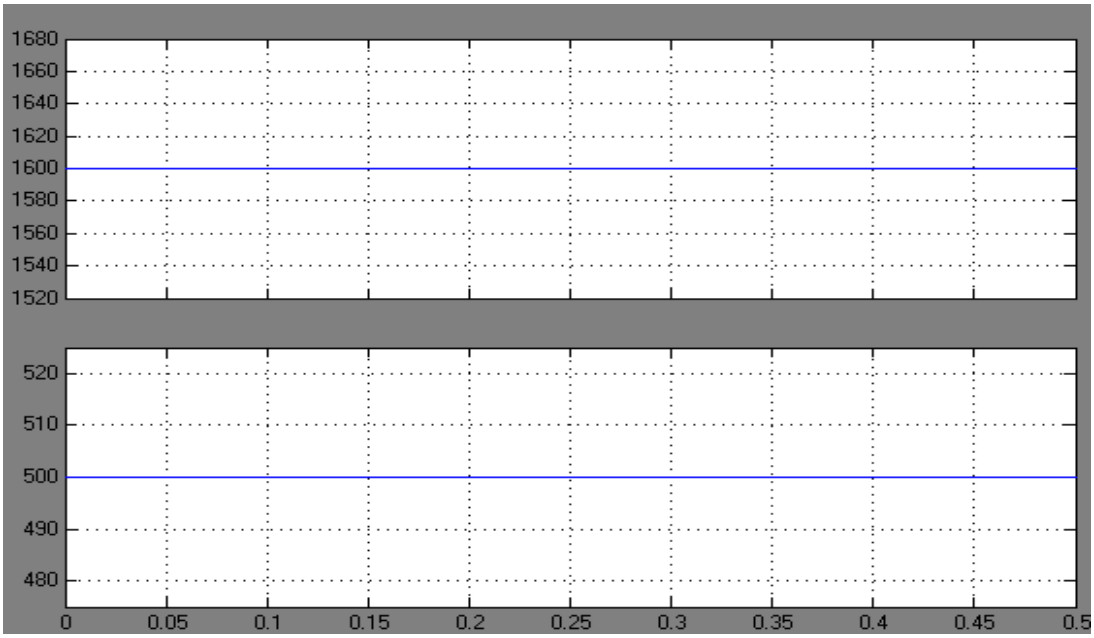

Fig. 6: Reactive power control of DC-link voltages of two inverters.

V. CONCLUSION

DC-link voltage parity is a standout amongst the significant issues over cascaded inverter-based STATCOMs. In this paper, a basic var compensating plan may be suggested to An cascaded two-level inverter- built multilevel inverter. Those plan ensures regulation for dc-link voltages of inverters at deviated levels What's more sensitive energy recompense. Those execution from claiming the scheme will be approved by reenactment under adjusted What's more lopsided voltage states. Further, the cause for precariousness when there is An change over reference current is

investigated. The progressive model may be formed What's more exchange capacities would determined. From those analysis, it will be inferred that those framework will be An non-minimum stage type, that is, poles of the exchange work generally lie on the exited A large portion of the plane. However, zero movement of the correct a large portion of the s-plane for certain working states. To such an system, oscillatory precariousness to helter skelter controller additions exists. By both dynamic Furthermore sensitive control the hysteresis misfortunes would diminished What's more effectiveness is expanded Similarly as recreated in MATLAB.

REFERENCES

[1] N. G. Hingorani and L. Gyugyi*, Understanding FACTS*. Delhi, India: IEEE, 2001, Standard publishers distributors.

[2] B. Singh, R. Saha, A. Chandra, and K. Al-Haddad, "Static synchronous compensators (STATCOM): A review," *IET Power Electron.*, vol. 2, no. 4, pp. 297–324, 2009.

[3] H. Akagi, H. Fujita, S. Yonetani, and Y. Kondo, "A 6.6-kV transformer less STATCOM based on a five-level diode-clamped PWM converter: System design and experimentation of a 200-V 10-kVA laboratory model," *IEEE Trans. Ind. Appl.*, vol. 44, no. 2, pp. 672–680, Mar./Apr. 2008.

[4] Y. Liu, A. Q. Huang, W. Song, S. Bhattacharya, and G. Tan, "Small signal model-based control strategy for balancing individual dc capacitor voltages in cascade multilevel inverter-based STATCOM," *IEEETrans. Ind. Electron.*, vol. 56, no. 6, pp. 2259–2269, Jun. 2009.

[5] H. P.Mohammadi and M.T. Bina, "Atransformerless medium-voltage STATCOM topology based on extended modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1534–1545, May 2011.

[6] X. Kou, K. A. Corzine, and M. W. Wielebski, "Over distention operation of cascaded multilevel inverters," *IEEE Trans. Ind. Appl.*, vol. 42, no. 3, pp. 817–824, May/Jun. 2006.

[7] K. K. Mohaptra, K. Gopakumar, and V. T. Somasekhar, "A harmonic elimination and suppression scheme for an open-end winding induction motor drive," *IEEE Trans. Ind. Electron.*, vol. 50, no. 6, pp. 1187–1198, Dec. 2003.

[8] Y. Kawabata, N. Yahata,M. Horii, E. Egiogu, and T. Kawabata, "SVGusing open winding transformer and two inverters," in *Proc., 35th AnnualIEEE Power Electron. Specialists Conf.*, 2004, pp. 3039–3044.

[9] S. Ponnaluri, J. K. Steinke, P. Steimer, S. Reichert, and B. Buchmann, "Design comparison and control of medum voltage STATCOM with novel twin converter topology," in *Proc., 35th Annu. IEEE Power Electron.Specialists Conf.*, 2004, pp. 2546–2550