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Compensation Strategy of voltage unbalance in Islanded Micro grids

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Abstract

In this paper, a control technique with low data transfer capacity correspondences for paralleled three-stage inverters is proposed to accomplish acceptable voltage unbalance remuneration. The proposed control calculation primarily comprises of voltage/current inner loop controllers, a droop controller, a specific virtual impedance circle, and an unbalance compensator. The internal circle controllers depend on the stationary reference casing to better mitigate the voltage twisting under nonlinear loads. Droop control and specific virtual impedance circle accomplish precise current-sharing when supplying both straight and nonlinear loads. In addition, by altering voltage references according to the sufficiency of the negative arrangement voltage, the unbalance variable, which is for the most part brought about by single phase generators/loads, can be moderated to a to a great degree low esteem.

I. INTRODUCTION

Lately, dispersed energy resources (DERs, for example, wind turbines, photovoltaic systems and micro-turbines, have pick up an awesome expanding enthusiasm since they are monetary and environment well disposed. When all is said in done, power electronic converters are utilized as interfaces amongst DERs and the lattice, such that electrical power with great quality and high dependability can be conveyed to the heap or utility matrix, as appeared in Fig. 1. This paper concentrates on islanded

micro grids where the interfacing converters primarily work as voltage sources to take an interest on the voltage and recurrence control while sharing at the same time active and reactive power precisely by conforming outputvoltage phase angles and amplitudes. Be that as it may, it is too favored that those converters could give power quality administration capacity, in a manner that we can take full utilization of the converters accessible limit. It is surely understood that power quality issues, particularly voltage/current unbalances and voltage/current mutilations have turned out to be increasingly genuine in present day power system. Case in point, in islanded micro grids, the voltage unbalance issue is a striking issue principally delivered by the utilization of single-stage generators/loads and it can lead to unsteadiness and power quality issues.

In order to enhance the voltage waveform quality, several components to deal with the voltage unbalance compensation

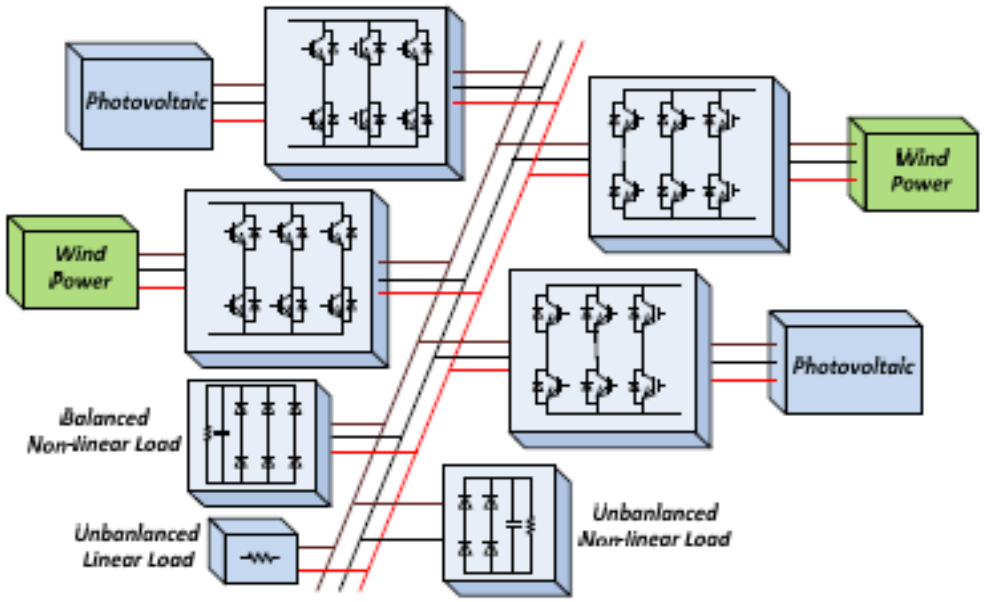


Fig. 1. General architecture of a micro grid

Have been created, for example, static var compensator (STATCOM) , arrangement active power channel and shunt dynamic power channel. Be that as it may, all these pay techniques use extra power converters to infuse negative succession reactive power. Just a couple works remunerate the unequal voltage by using the DG interfacing converters. The DG inverter is controlled to infuse negative arrangement current to equalization the basic bus voltage. Be that as it may, a surplus converter limit is expected to produce the negative succession current what's more; the infusing current may be too high under serious unbalance conditions. In the past work, an unbalance pay technique is proposed by sending appropriate control signs to DGs neighborhood controllers. In any case, the negative arrangement segment of the

normal transport voltage is difficult to smother, following the micro grid central controller (MGCC) employments the voltage unbalance element as a fundamental control variable, which quality is diminished by the positive arrangement voltage.

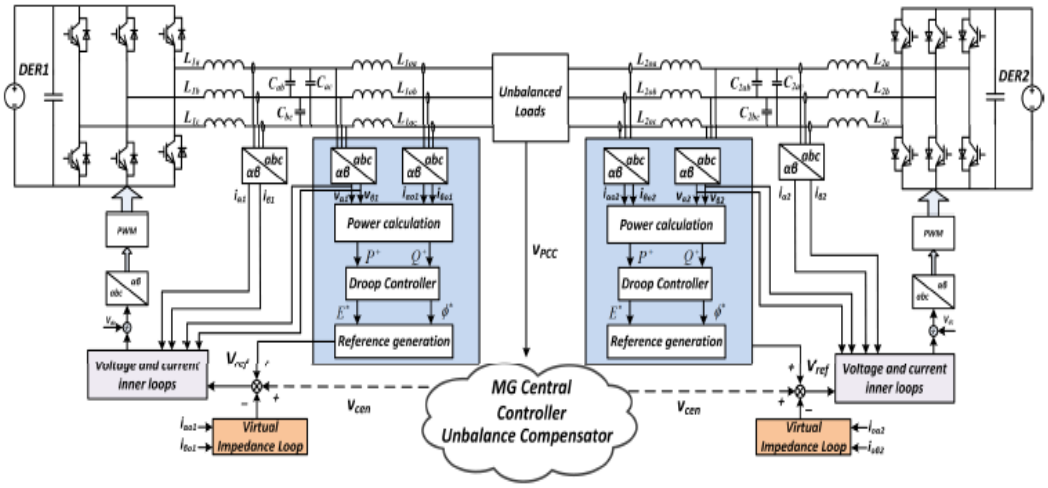


Fig. 2. Implementation of the local controllers.

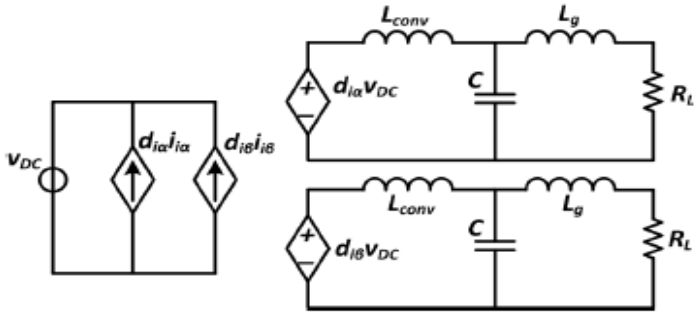


Fig. 3. Small signal model of single inverter.

II. LOCAL CONTROLLER DESIGN

Fig. 2 delineates the control system of inverter nearby controllers. LCL channel is received here; however it really works as a routine LC channel with a coupling inductor. The principle capacity of the system side inductor is to enhance the element execution and to shape the output impedance. Additionally its current is measured for force figuring and virtual impedance which will be clarified later.

A. Inner Loop Design

It can be seen from Fig. 2 that the inner loops are executed in two-stage stationary casing and all the measured voltage and current are changed from abc to αβ organizes,

in this manner the computational weight is decreased altogether. Both voltage and current controllers depend on proportional resonant (PR) controller rather than the customary proportional integrator (PI) controller. The reason is that PR controller can give unending addition at the chosen full recurrence to give tasteful following execution. As it were, the execution of PR controller at chose full resonant frequency like the execution of PI controller at 0Hz. Additionally, keeping in mind the end goal to mitigate the voltage and current bending under nonlinear loads, the PR controllers are tuned at essential frequency,3rd, 5th, 7th, 9th and 11th order harmonics.

$$v_c(s) = v_o^*(s) - Z_o(s) i_o(s) = \frac{G_v(s) G_i(s) G_{PWM}(s)}{LCs^2 + CG_i(s) G_{PWM}(s) s + G_v(s) G_i(s) G_{PWM}(s) + 1} v_{ref}(s) - \frac{Ls + G_i(s) G_{PWM}(s)}{LCs^2 + CG_i(s) G_{PWM}(s) s + G_v(s) G_i(s) G_{PWM}(s) + 1} i_o(s) \quad (1)$$

where vc(s) is the capacitor voltage, v*o (s) is the open circuit voltage, io(s) is the output current, Zo(s) is the equivalent output impedance, vref(s) is the voltage reference, L is the converter side inductor, C is the filter capacitor. Gv(s), Gi(s) and GPWM(s) are the transfer function of voltage controller, current controller and PWM delay, respectively. Their transfer function can be expressed as:

$$G(s) = k_{vp} + \sum_{h=1,3,5,7,9,11} k_{hvr} \frac{s}{s^2 + (h\omega)^2} \quad (2)$$

$$G(s) = k_{ip} + \sum_{h=1,3,5,7,9,11} k_{hir} \frac{s}{s^2 + (h\omega)^2} \quad (3)$$

$$G_{PWM}(s) = \frac{1}{1 + 1.5 T_s s} \quad (4)$$

B. Droop Control Implementation

With a specific end goal to abstain from circling streams among the parallel inverters without utilizing correspondence join between them, droop control is embraced in this paper. To better shows hang control hypothesis, accepting two inverters associated in parallel and sharing loads at the normal node. The equal circuit is appeared in Fig. 6. From Fig. 6, the dynamic force P and reactive power Q infused by every DG can be express in (5) and (6), separately.

$$P_i = \left(\frac{E_i V}{Z_i}\cos\varphi_i - \frac{V^2}{Z_i}\right)\cos\theta + \frac{E_i V}{Z_i}\sin\varphi_i \sin\theta \quad (5)$$

$$Q_i = \left(\frac{E_i V}{Z_i}\cos\varphi_i - \frac{V^2}{Z_i}\right)\sin\theta - \frac{E_i V}{Z_i}\sin\varphi_i \cos\theta \quad (6)$$

Where Ei and φi are the sufficiency and the stage point of the output voltage of the every inverter, Zi and θi are the sufficiency also, stage point of the line impedance of every inverter, individually. V is the voltage amplitude of regular AC bus.
Note that stage edge of regular AC bus voltage is taken as the stage reference. As a rule, the line impedance is for the most part inductive, i.e. 90 i Z ∠θ ≈ X ∠ °. Moreover, expecting the stage contrast φi between inverter voltage and AC transport voltage is little enough, so that sinφi can be around equivalent to φi and cosφi can be around equivalent to 1. At that point, from (5) and (6), the accompanying approximations can be acquired:

$$P_i \approx \frac{E_i V}{X_i}\varphi_i \quad (7)$$

$$Q_i \approx \frac{E_i V}{X_i}\sin\theta - \frac{V^2}{X_i} \quad (8)$$

From (7) and (8), it can be seen that active power Pi is predominant by phase angle φi while reactive power is for the most part rely on upon inverter voltage Ei. At that point, a fake droop is acquainted here with change the frequency and amplitude of the output voltage powerfully:

$$\varphi^* = \varphi_0 - \left(m_p + \frac{m_I}{s}\right)\left(P^+ - P^+_{ref}\right) \quad (9)$$

$$E^* = E_0 - n_p\left(Q^+ - Q^+_{ref}\right) \quad (10)$$

where φ* and E* are the sufficiency and stage point of the output voltage reference while E0 and φ0 are the sufficiency and phase angle of the output voltage at no load condition, P+ and Q+ are the momentary principal positive succession dynamic what's more, reactive power, individually, and P + ref are Q+ ref are the reference of central positive arrangement active and reactive power, individually; mp and mI are the corresponding and essential coefficients of dynamic force controller, separately. mI chiefly impact the dynamic normal for the system since it includes latency to the system; np is the essential coefficients of reactive power controller.

It can be seen from (7)- (10) that the higher the droop coefficients is, the better power sharing can be achieved. Be that as it may, the voltage and frequency deviation will likewise get to be bigger when the droop coefficients get to be greater. This tradeoff can be repaid by presenting optional controller, as represented. Henceforth, both the corresponding coefficients ought to be precisely chosen by and (12):

$$m_p = \frac{\Delta f}{P} \tag{11}$$

$$n_p = \frac{\Delta E}{Q} \tag{12}$$

Where Δf and ΔE are the most extreme suitable deviation of frequency and amplitude from its ostensible worth, separately. P and Q are the appraised dynamic and responsive force, separately. A positive-negative-succession consonant voltage/current segment extractor in view of a second-order generalized integrator (SOGI) is actualized to help the droop controller and the virtual impedance circle, which will be presented in Section C. Since the key positive grouping part extraction is just about the same with that of the key negative grouping and music, just the key positive grouping voltage extractor is appeared here in Fig. 7.

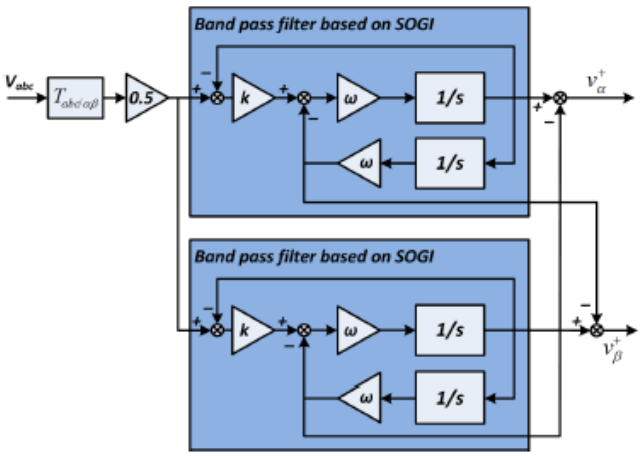


Fig. 7. Fundamental positive sequence component extractor.

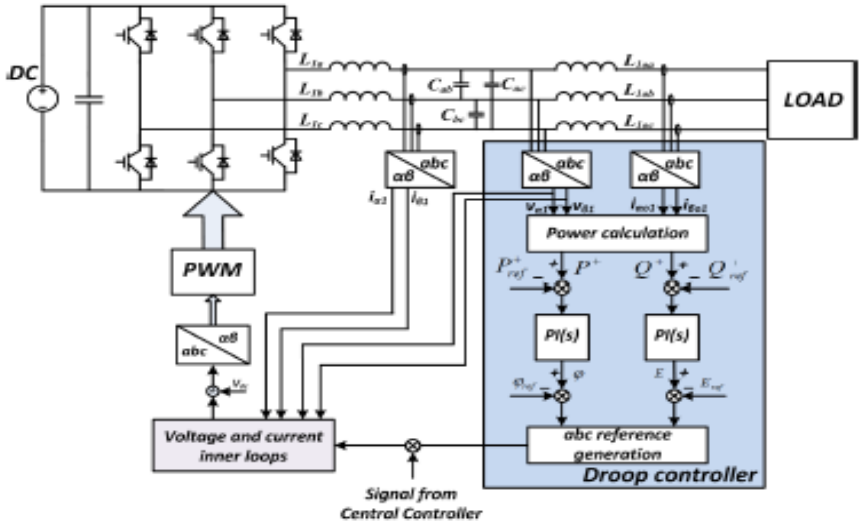


Fig. 8. Implementation of the droop controller.

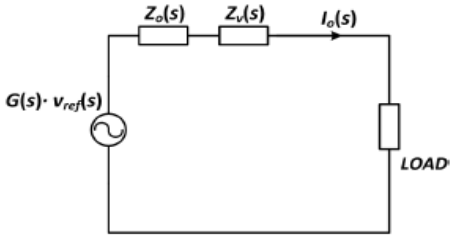
Fig. 8 delineates the execution piece graph of the droop controller. The power count piece, in view of the instantaneous reactive power hypothesis, is trailed by a low pass channel with a 2 Hz cut-off frequency, so that the force swaying can be sifted through.

C. Virtual Impedance Loop

Keeping in mind the end goal to share the force decisively between the circulated inverters, the output impedance of the inverter must be re-intended to alleviate the impact of control parameters what's more, line impedance on the power sharing exactness. Here, (1) can be revamped as:

$$v_c(s) = G(s)v_{ref}(s) - Z_o(s)i_o(s) \qquad (13)$$

Where G(s) speaks to the nearby circle exchange capacity of the inverter, and Zo(s) speaks to the nearby circle output impedance of the inverter. From the above condition, a two-terminal Thevenin comparable circuit of the nearby circle inverter can be gotten, as appeared in Fig. 9.



If no control loop is implemented to compensate the output impedance, the amplitude of the output impedance at fundamental frequency and 3rd, 5th, 7th, 9th and 11th order harmonics is extremely small, as shown the blue curve in Fig. 10. Thus, a virtual impedance loop must be added in the control block to fix the output impedance.

Since the droop law in this paper is ensured just when the output impedance is exceedingly inductive. In this manner, a positive sequence virtual inductor L + v is added to make the output

Impedance more inductive, so a superior decoupling of P and Q can be guaranteed. The reason for including the positive-arrangement energy resistor R+ v is to make the system more damped, so that the output current can be constrained inside a satisfactory reach.
For basic negative sequence and every request of the sounds, a resistor is imitated at the output side to upgrade the sharing of nonlinear load sharing among the DGs. Contrasted and utilizing a real resistor, the virtual resistor has the point of preference of no power losses and the likelihood to choose sounds and sequences.
The execution plan of the virtual impedance circle, which comprises of three principle parts, is represented in Fig. 11. The initial segment is central positive grouping virtual impedance circle, which just presents virtual resistor R+ v and virtual inductor L + v to crucial positive sequence current. The second part is fundamental negative sequence virtual impedance circle which presents virtual resistor R − v to crucial negative succession current. The third part is consonant virtual impedance loop which presents energy resistor Rh to 3rd, 5th, 7th, 9th and 11th order harmonics, individually. Note that ω is the nominal angular frequency of the system.
It is important that there is a tradeoff between the nonlinear current sharing precision and inverters output voltage twisting. This voltage contortion begins from the voltage drop on the virtual impedances. In this manner, the estimation of the virtual impedances must be chosen deliberately to guarantee a well power sharing precision, and in the interim ensure the voltage Total Consonant Distortion (THD) is constrained in an adequate reach. Moreover, voltage contortion brought about by virtual impedance is additionally the purpose behind isolating the virtual impedance of consonant and central negative arrangement part with crucial positive succession part, so that the virtual impedance of crucial negative succession and consonant parts can be set to a larger quality.

III. UNBALANCE COMPENSATOR DESIGN

In this paper, the voltage unbalance remuneration technique is enhanced regarding controlling the negative sequence voltage specifically. As appeared in Fig. 2, the reference of voltage controller is the superposition of the output of unbalance compensator and droop controller. The numerical portrayal of the unbalance compensator actualized in synchronous reference (dq) frame is appeared in (14):

$$v_{cen} = \left[\left(\left| v^- \right|_{ref} - \sqrt{v_d^{-} + v_q^{-}} \right) \cdot PI_1(s) - Q^- \right] \cdot PI_2(s) \cdot \frac{v_{dq}^-}{\sqrt{v_d^{-} + v_q^{-}}} \quad (14)$$

Where vcen is the control signal sends to inverter neighborhood controller, $|v^-|_{ref}$ is the reference of negative arrangement voltage Q^- is the negative arrangement reactive power at purpose of basic coupling (PCC), v_d^- and v_q^- are the dq segments of negative arrangement voltage separately, PI1(s) and PI2(s) are the negative succession voltage controllers, individually. It can be seen that the voltage unbalance level is relieved by controlling the PCC voltage straightforwardly while the negative arrangement receptive power infusion is controlled in a roundabout way.

Extension

Multi level inverter

Various mechanical applications have started to require higher force contraption as of late. Some medium voltage engine drives and utility applications require medium voltage and megawatt power level. For a medium voltage framework, it is troublesome to interface stand out force semiconductor switch specifically. Therefore, a multilevel force converter structure has been presented as an option in high power and medium voltage circumstances. A multilevel converter accomplishes high power appraisals, as well as empowers the utilization of renewable vitality sources. Renewable vitality sources, for example, photovoltaic, wind, and energy units can be effortlessly interfaced to a multilevel converter framework for a powerful application.

The term multilevel started with the three-level converter. In this manner, a few multilevel converter topologies have been created. Be that as it may, the rudimentary idea of a multilevel converter to accomplish higher force is to utilize a progression of force semiconductor switches with a few lower voltage dc sources to play out the force change by integrating a staircase voltage waveform. Capacitors, batteries, and renewable vitality voltage sources can be utilized as the different dc voltage sources. The substitution of the force switches total these numerous dc sources with a specific end goal to accomplish high voltage at the yield; be that as it may, the appraised voltage of the force semiconductor switches depends just upon the rating of the dc voltage sources to which they are associated.

A multilevel converter has a few points of interest over an ordinary two-level converter that utilizations high exchanging recurrence beat width regulation (PWM). The appealing elements of a multilevel converter can be quickly compressed as takes after.

- Staircase waveform quality: Multilevel converters not just can produce the yield voltages with low contortion additionally can diminish the dv/dt stresses; along these lines electromagnetic similarity (EMC) issues can be decreased.
- Common-mode (CM) voltage: Multilevel converters produce littler CM voltage; along these lines, the anxiety in the direction of an engine associated with a multilevel

engine drive can be diminished. Moreover, CM voltage can be wiped out by utilizing propelled tweak techniques, for example, that proposed.

- Input current: Multilevel converters can draw info current with low twisting.
- Switching recurrence: Multilevel converters can work at both principal exchanging recurrence and high exchanging recurrence PWM.

Fig. 13. PCC voltages

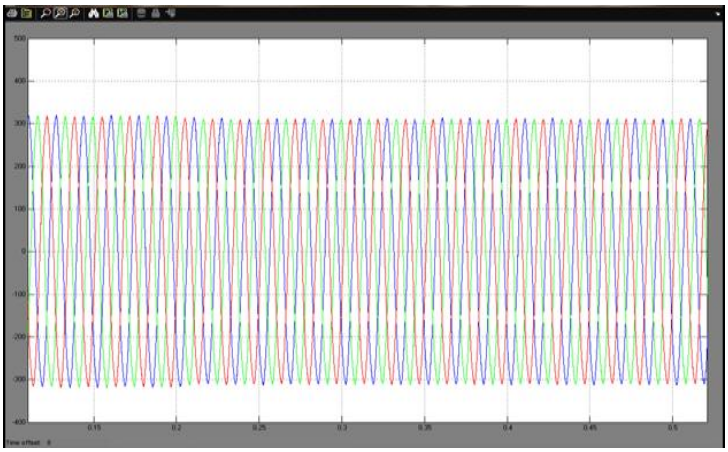


Fig. 14. PCC voltage unbalance factor.

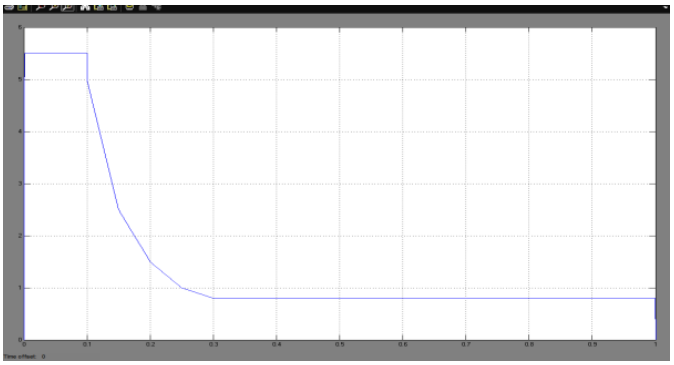
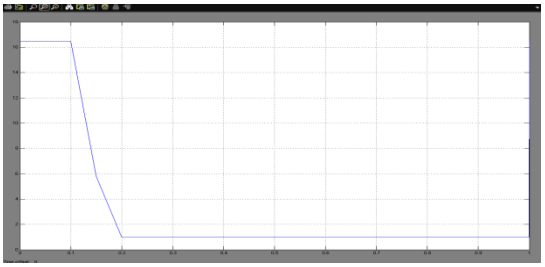


Fig. 15. Negative sequence voltage of PCC.

Vd.



Vq.

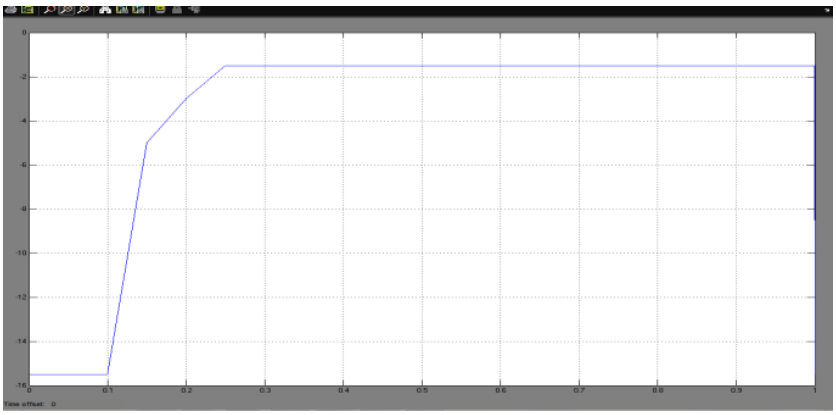
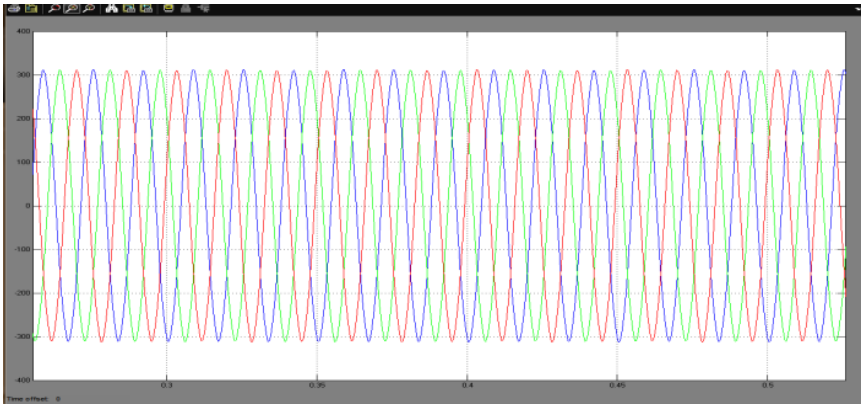


Fig. 16. Output voltage of DG1, DG2.



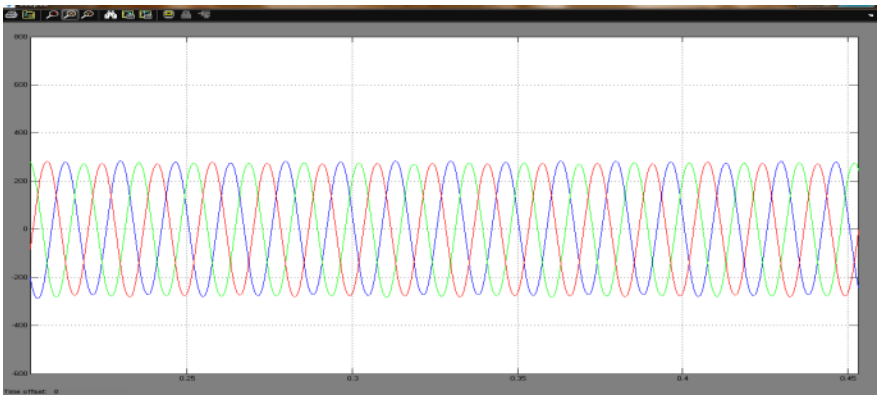
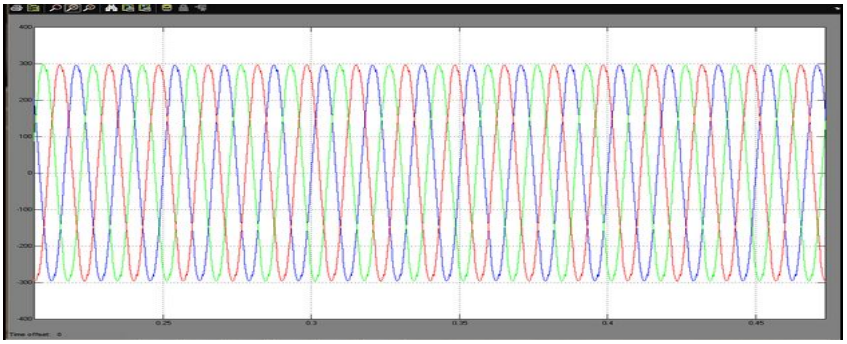
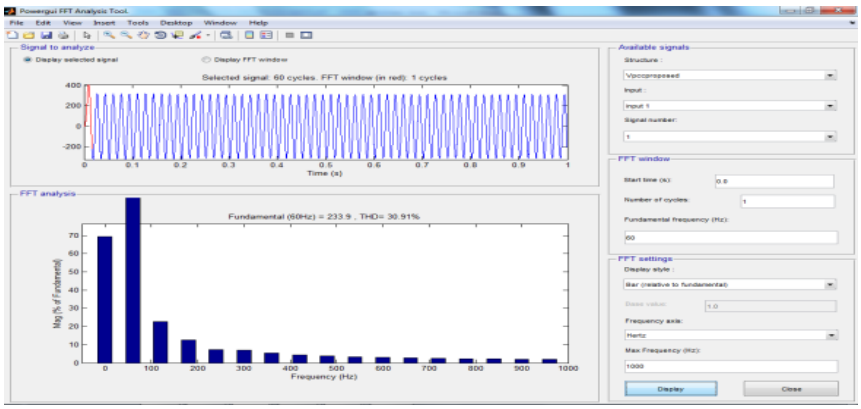


Fig. 13. PCC voltages after compensation



THD for Vpcc for both proposed & extension are:
Proposed THD:



Extension THD:

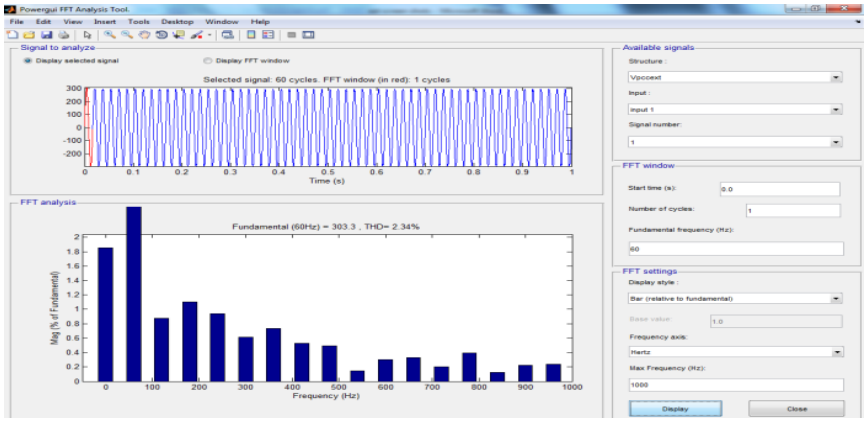


Fig. 17. Output current of DG1, DG2

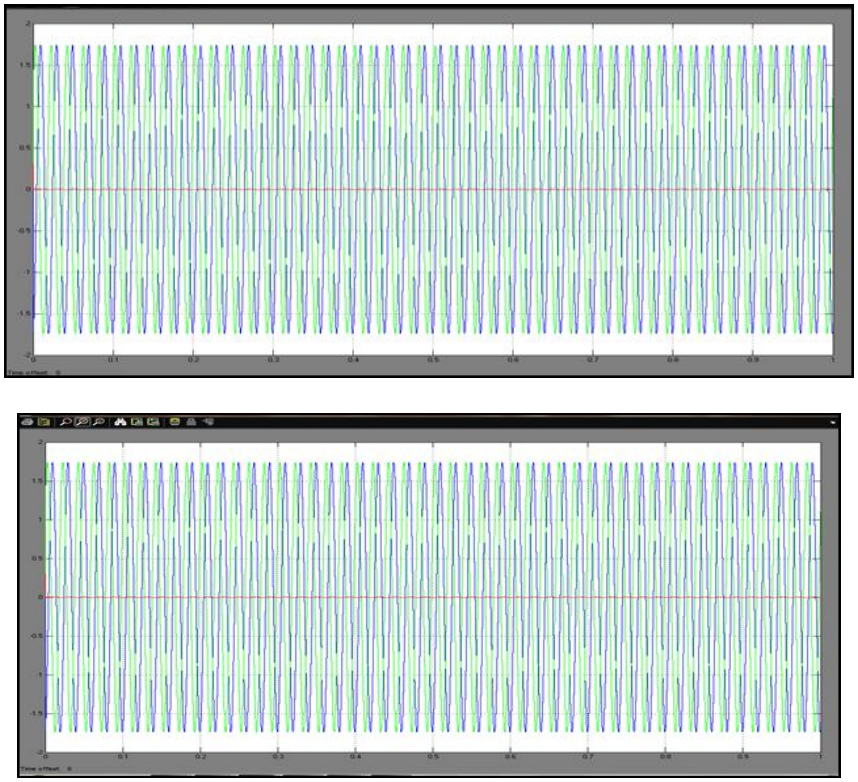
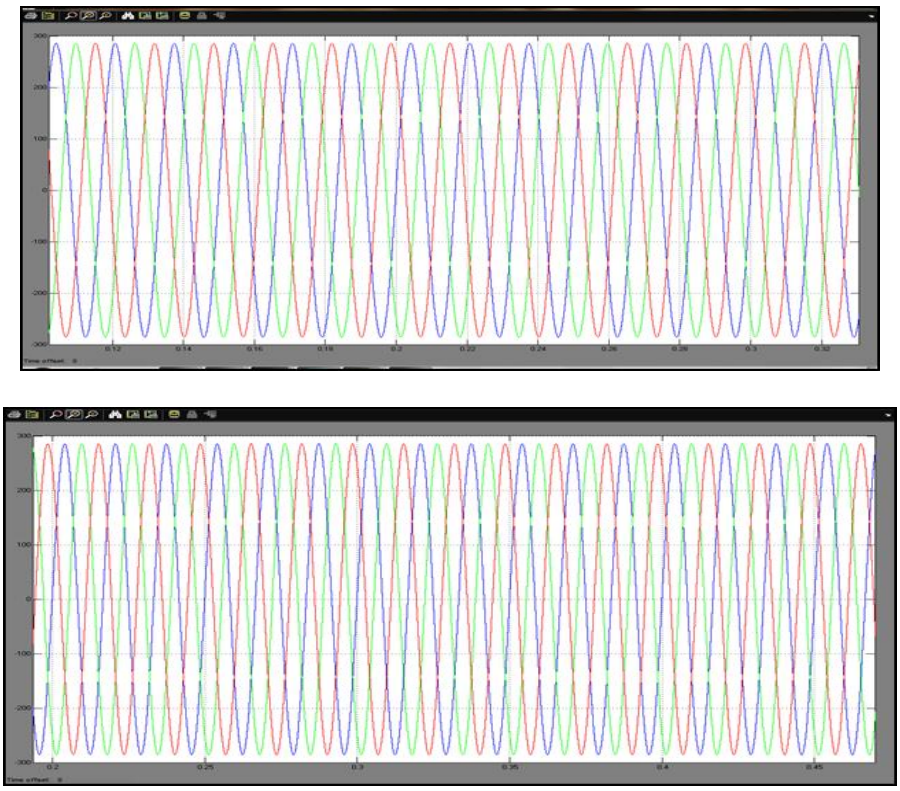
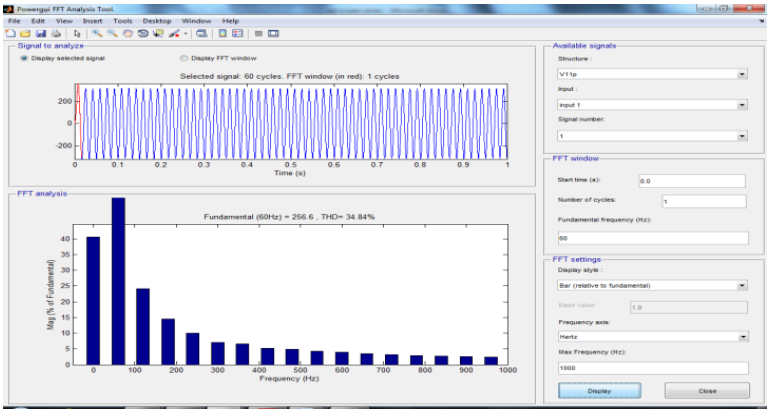
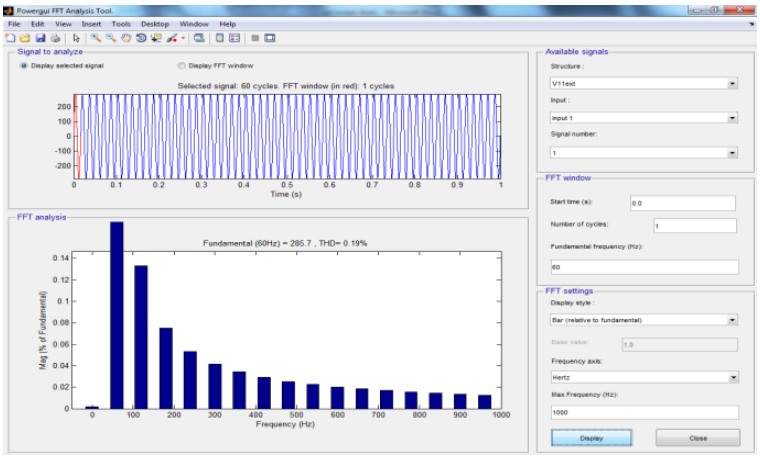


Fig. 16. Output voltage of DG1, DG2.

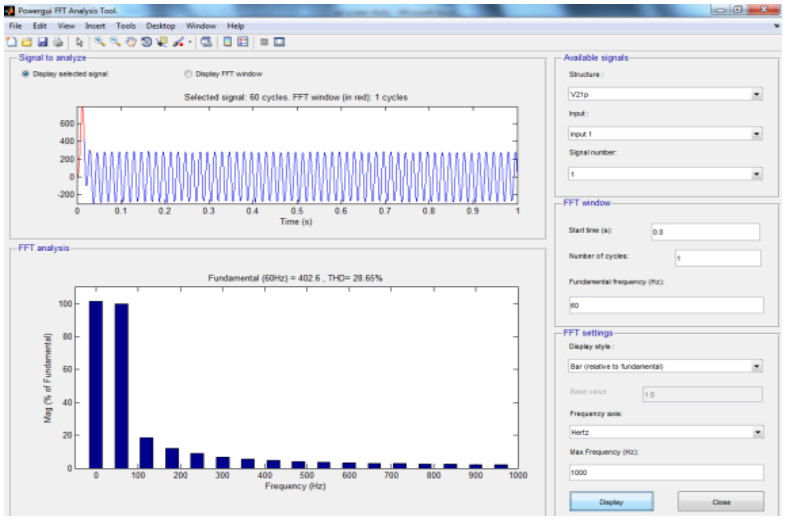


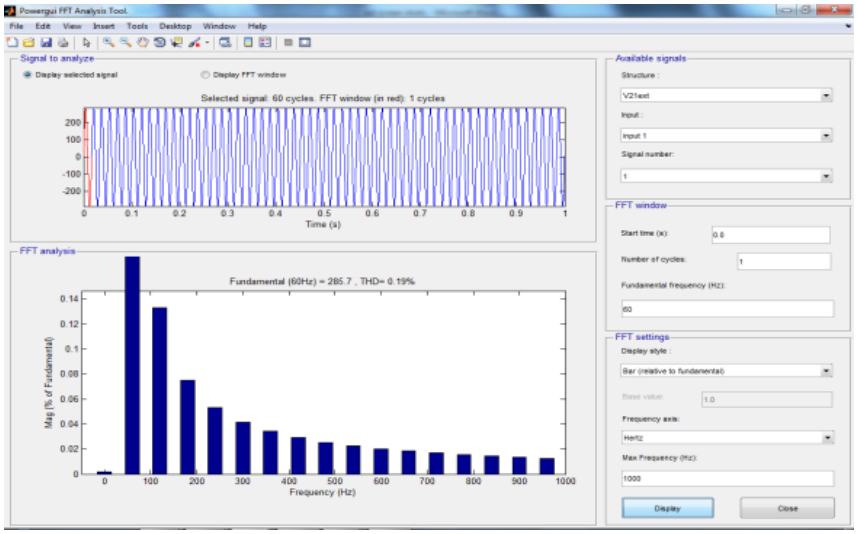
THD's for output voltages of DG1 under proposed and extension are:





THD for Output voltage of DG2 under proposed & extension are:





CONCLUSION

In this paper, a novel direct voltage unbalance pay control system for islanded micro grids has been researched. The control structure incorporates two levels: a neighborhood controller and an immediate voltage unbalance compensator. The neighborhood controller for the most part deals with the transport voltage direction furthermore, the power sharing exactness, while the immediate voltage unbalance compensator adds to relieve the voltage unbalance at the PCC by controlling the voltage reference. The effectiveness of the control plan has been approved with three LCL DG converters connected in parallel sharing a normal AC bus. The exploratory results demonstrate that the negative grouping voltage can be all around stifled to the desired worth with a fulfilled load sharing accuracy.

REFERENCES

[1] H. Nikkhajoei and R.H. Lasseter, "Distributed generation interface to the CERTS micro grid," IEEE Trans. Power Del., vol. 24, no. 3, pp. 1598- 1608, Jul. 2009.

[2] Y. Xu, L.M. Tolbert, J. D. Kueck, and D.T. Rizy, "Voltage and current unbalance compensation using a static var compensator," IET on Power Electron., vol. 3, no. 6, pp.977-988, Nov. 2010.

[3] P. S. Flannery, G. Venkataramanan, "Unbalanced voltage sag ride through of a doubly fed induction generator wind turbine with series grid-side converter," IEEE Trans. on Ind. Appl., vol. 45, no. 5, pp. 1879- 1887, Sep.-Oct. 2009.

[4] Y. Xu; L. M. Tolbert, and J. D. Kueck, "Voltage and current unbalance compensation using a parallel active filter," IEEE Power Electron. Spec. Conf., pp. 2919-2925, June 2007.

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